Challenges of Monolithic MEMS-on-CMOS Integration for Spatial Light Modulators

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ABSTRACT

The development of devices that are based on MEMS-on-CMOS technology becomes increasingly time-consuming since System-on-a-Chip (SoC) solutions for highly integrated and miniaturized devices are approaching smaller feature sizes. In order to reduce the development costs and shorten the time-to-market periods, the combination of commercially available CMOS processes from foundries with the subsequent processing in a dedicated MEMS facility is beneficial. This concept offers the possibility to separate the different technological requirements of conventional CMOS manufacturing and MEMS actor processing, which may follow different design rules and process specifications. As a representative of the dedicated MEMS foundries, Fraunhofer IPMS performs surface micromachining on 200 mm wafers for a variety of MEMS devices, in particular for spatial light modulators (SLM). Over the past decade, much experience was gained in development activities for customer specific applications like micro mirror arrays.

In this paper, we will discuss essential requirements and upcoming challenges for the monolithic integration of surface micro-machined optical MEMS on foundry-fabricated CMOS backplanes, as conventional (i-Line) lithography is approaching patterning limits. We will present approaches of tuning the planarization of the CMOS chip surface to achieve an excellent mirror array flatness with CMOS compatible inorganic sacrificial layer techniques. Concepts like Mix&Match lithography for achieving high overlay accuracy and the litho stitching technique for the patterning of large chips will be reviewed and a brief outline of our roadmap for the implementation of DUV lithography will be presented.

Keywords: SLM, Spatial Light Modulators, MEMS-on-CMOS, CMOS Backplanes, Monolithic Integration

1. INTRODUCTION

The spatial light modulators developed at Fraunhofer IPMS consist of micro mirrors arrays (MMA) on semiconductor chips, whereby the number of mirrors varies depending on the application, from a few hundred to several millions. In most cases this requires a highly integrated application-specific electronic circuit (ASIC) as basis for the component architecture in order to enable an individual analog or binary / digital deflection of each micro mirror. In addition, Fraunhofer IPMS develops the external drive electronics and software for data transfer and control of the MMAs.

The individual mirrors that vary in number and size per chip can be either tilted or vertically deflected depending on the application, so that a surface pattern is created, for example to project defined structures. High-resolution tilting mirror arrays with up to 2.2 million individual mirrors are used by our customers as highly dynamic programmable masks for optical micro-lithography in the ultraviolet spectral range [1]. The mirror dimensions typically are 10 µm or larger (Figure 1, [2]). By tilting individual micro mirrors, lateral information is transferred to a high-resolution photo resist at high frame rates. Further fields of application are mask inspection and measurement technology for the semiconductor industry, microscopy and prospectively laser printing, marking and material processing.

Piston micro mirror arrays can for example be used for wavefront control in adaptive optical systems. These systems can correct wavefront disturbances in broad spectral ranges and thereby improve image quality. The component capabilities attract special interest in the fields of ophthalmology, astronomy and microscopy, as well as in spatial and temporal laser beam and pulse shaping [3].

Figure 1: Ceramic-packaged 48µm, 512 x 320 Tip-Tilt micro mirror array with a programmed pattern (right) [2].

2. MEMS-ON-CMOS INTEGRATION CHALLENGES

2.1 Integration Concepts

There are various methods of combining MEMS and CMOS properties in a device such as (heterogeneous) multi-chip and multi-wafer integration. This paper is focused on the monolithic integration of MEMS on CMOS backplane wafers. A large number of MEMS technologies are realized at Fraunhofer IPMS using this MEMS-last approach such as micro-mirror arrays, infrared bolometers, inertial sensors or bulk acoustic wave resonators [4-7]. The most important advantage of this integration concept is that standard foundries can be utilized to fabricate the CMOS backplanes with the flexible choice of technology nodes. MEMS structures are then fabricated on top of the CMOS wafers in a dedicated MEMS fab such as IPMS.

Fraunhofer IPMS comprises a 1500m^2 class 10 (iso4) FEoL cleanroom for 200mm wafer processing. Classical MEMS manufacturing technologies such as surface and bulk micromachining, sacrificial layer and release technologies as well as a multitude of specialized PVD / CVD, CMP and litho/etch processes are used to generate MEMS and MOEMS devices at highest integration levels. Figure 2 gives a schematic of such a monolithically integrated micro mirror array (MMA) on top of a CMOS cell including interconnect layers, driving electrodes and the flexible MEMS layers (hinge, mirror). Significant challenges arise when adjusting the MEMS processes to the CMOS device.

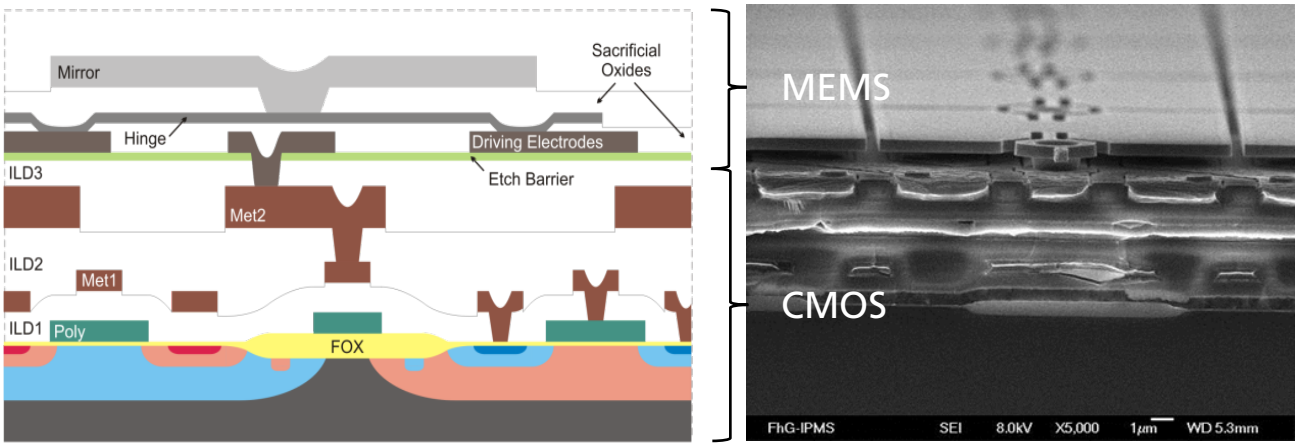


Figure 2**:** Schematics of monolithic integration and an example for a Micro Mirror Array (SLM)

2.2 CMOS Backplane planarity

A planar CMOS wafer surface facilitates the integration of the MEMS part. Planarity is required to ensure the functionality of the MEMS devices since they are usually sensitive to in-plane distortions, even in the lower MEMS layers. It also helps in the reliable formation of the initial VIA openings across the wafer. In many cases it is beneficial to skip the opening of test pads for electrical reliability tests in the CMOS fab since these would have to be buried with oxide again before the MEMS processing, which impacts the chip planarity. Instead, electrical tests should be performed on representative wafers that are not further processed in the MEMS facility to avoid contamination with noble metals. However, if necessary, refilling and planarizing of open bond pads is possible but it requires some effort such as design specific inverse etching to obtain a good chip planarity (Figure 3).

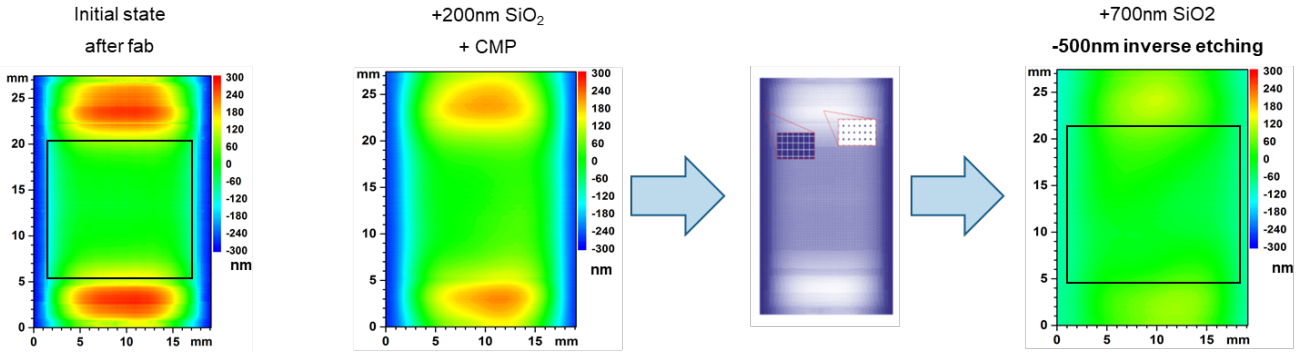


Figure 3: Initial chip planarity of a CMOS chip (left) and after subsequent CMP and layout-specific inverse etching steps to tune CMOS-Backplane Chip Topography. The bond pad areas are visible in the top and bottom part of the chip.

2.3 Layout

The layout of the CMOS wafer should consider the MEMS processing requirements. Areas for optical film thickness measurements should be kept free from underlying dummy structures such as CMP fill pattern to enable a reasonable analysis. Similarly, the blocking of the dummy structures is also necessary in areas that serve as alignment mark area in the MEMS part where dummy structures would obstruct the alignment (Figure 4). The area density of structures in the scribe line should also be close to that of structures in the chip area to enhance the chip planarity. Structures for the determination of the overlay accuracy should be present in the CMOS wafer to be able to match the MEMS lithography to that of the CMOS foundry.

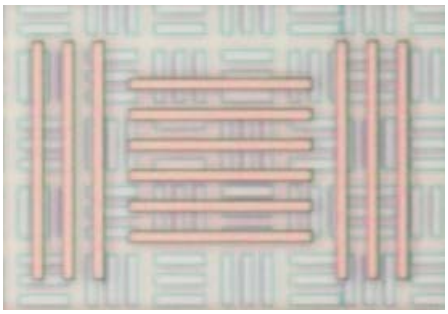
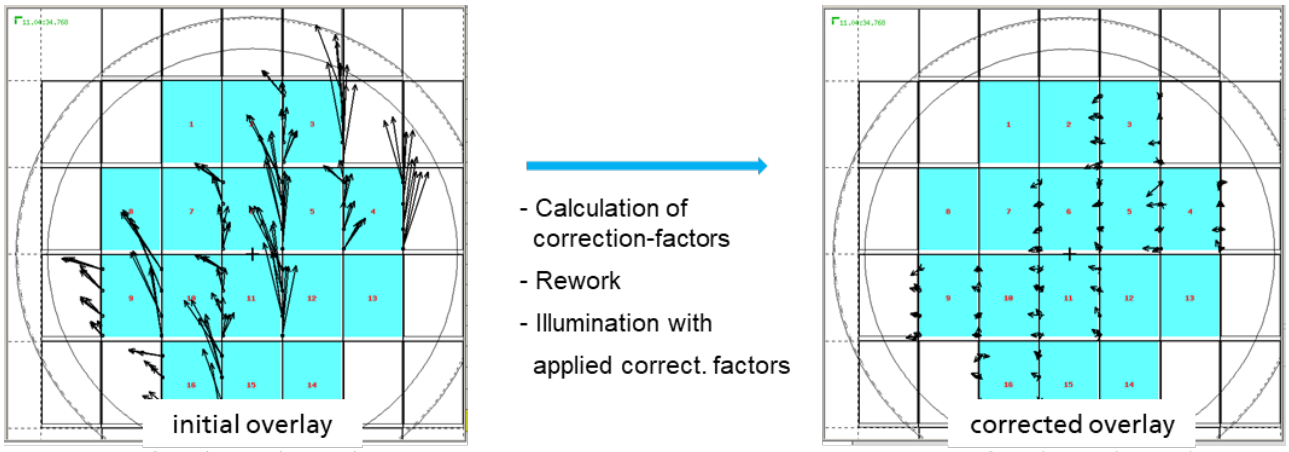


Figure 4: Example of STI dummy structures in a CMOS wafer obstructing stepper alignment marks in a MEMS layer.

Often, MEMS structures are processed using a number of sacrificial layers that are etched off during later stages of the production or after dicing. To prevent the etchants from damaging the CMOS part a chip sealing is necessary that reaches from the wafer substrate to the MEMS-layers. The choice of the sealing material depends on the kind of sacrificial layer that is used for the MEMS part. For oxide sacrificial layers that are removed via gas phase HF etching, an amorphous silicon (aSi), alumina, or metal sealing can be used to serve as the side-wall of the encapsulation. For other sacrificial layers different sealings are required. In most cases, the top-side sealing is formed during the MEMS processing and needs not to be considered in the CMOS part.

2.4 Mix&Match Lithography

An essential part of the MEMS-on-CMOS technology is an accurate Mix&Match lithography with high overlay accuracy between BEoL and FEoL layers. Insufficient accuracy might lead to MEMS structures standing on structural edges of underlying layers, which might become recognizable only in the end tests of the final device where a repair is no more possible. Using i-Line lithography and overlay measurements in combination with litho rework loops an accuracy of approximately 50 nm (stepper specs) can be achieved (Figure 5).



Property	Unit	Min.	Mean.	Max.
OVL (X)	nm	-90,6	-22,0	56,1
OVL (Y)	nm	6,8	93,1	182,2

Property	Unit	Min.	Mean.	Max.
OVL (X)	nm	-40,0	-4,0	24,0
OVL (Y)	nm	-31,1	-0,1	28,5

Figure 5: Correction of i-Line OVL mismatch using litho rework loops and run-to-run control.

2.5 CD-Uniformity

In the IPMS clean room an i-Line stepper (Nikon NSR-2205i14E2) is utilized. This stepper type uses a reduction ration of 5:1 and offers a maximum exposure field of 22mm on the product. Some products however require a much bigger chip size or pixel area. Therefore, stitching of various mask partitions is necessary for lithography. Choosing the optimal partition size often is a trade-off. On one hand side minimal exposure field size gains best possible CD-uniformity on the lithography mask. On the other hand, a maximum field size decreases the necessary number of shots per wafer and chip and thus reduces the processing time and the possible impact of shot-to-shot effects. Furthermore, a minimum size of the partition is necessary for using an appropriate number of the scanners focus sensors, enabling a reasonable focus and tilt correction.

A MMA-device has two layers or parts with critical dimensions. Firstly the hinge, whose width and thickness crucially defines the voltages necessary for the targeted deflection angles. While thickness (uniformity) is a matter of sputter deposition only, lithography influences the hinge width as well as metal etch process using reactive ion etching (RIE). The second critical dimension is the slit width between the single mirrors. Obviously it has to be as narrow as possible to obtain a high fill factor, which leads to best reflected intensity and contrast in the image plane. Further light passing the mirror slits can cause (de)charging effects on the various parts of the MMA or by multiple reflection also in the DRAM storage cells, resulting in an unstable mirror deflection angle. However, the slit width cannot be reduced to any size. One fact, which sets a lower limit is, that adjacent mirrors tilted against each other must not touch each other for given deflection angles. Depending on mirror size, gap height and pull-in angle a minimum CD for the mirror slit exists. However, to obtain best mirror planarity after manufacturing but also after long-term operation under high power light exposure, a minimum mirror thickness is necessary. Usually this mirror thickness is higher than the minimum slit width, leading to an aspect ratio of >2. Since RIE for metal etch has a relatively bad selectivity, the necessary resist thickness used for patterning mirrors is similar or even bigger than the mirror thickness itself, usually by factor 1.4. For the usual chip design, 2.8µm thick resist is used to pattern a target slit width of (1.0±0.2)µm into 2.0µm thick mirrors. This combination sets enormous demands on lithography and RIE since optical resolution is very important here, even when

the absolute CD value is much bigger than pure i-Line resolution. One might think about using some kind of hard mask instead of resist. However, standard material for such hard mask would be SiO_2 deposited by CVD, which is a process at elevated temperatures that usually exceed the temperature limit of the mirror material. The mirror consists of a metal stack with a TiAl core, which is stress adjusted to optimize mirror planarity. Exposing the mirror to higher temperatures would change the stress of the mirror materials as described in [8,9] and drastically disturb the mirror planarity. Additionally, removing such a hard mask leads to the problem, that any etching before the final mirror release would attack the sacrificial layer and possibly the mirror too. But any removal during the final release by vaporous HF [10] could then lead to various types of residues [11,12] not only underneath the mirrors but also on its surface. Therefore, etching with a resist mask still is the best option here. A simplified schematic of the standard process flow is shown in Figure 6.

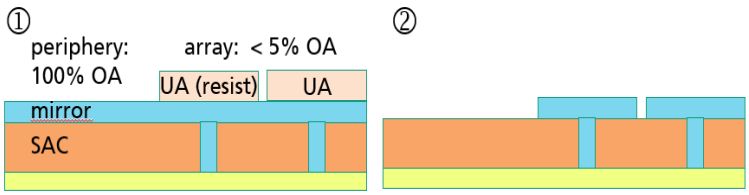


Figure 6: Process flow for standard process using only a single litho/etch sequence for mirror patterning. 1: After lithography. 2: After RIE for patterning of the mirror slits and removal of the mirror material in the periphery.

Using such a standard process would work for many layers, however for mirror slits it has a great drawback. The chip area can be separated into two domains, the pixel area and the periphery. A standard one step litho-etch sequence would etch the 1.4µm mirror slits into 48µm pixels, while simultaneously the complete mirror material in the periphery is removed. Obviously, there is a huge difference in the open area (OA) of the resist mask for the two domains, ~3% in the pixel areas versus 100% in the periphery. Thus, profile micro loading as well as aspect ratio dependent etch (ARDE) effects adversely influence the CD [13], leading to a long-range proximity effect at the boarder of the pixel area. Figure 7 shows the wafer map of the mirror slit width as measured by a CD-SEM (AMAT Verity 2) with 40 measurement points per chip. The specification of the slit width is still fulfilled, however it is clearly visible that especially within a single chip there is a big CD variation from edge (low CD) to center (high CD). The range of this effect extends several millimeters. Since the chip is litho stitched, it is obvious that the observed non-uniformity here is purely caused by the etching step and not by lithography.

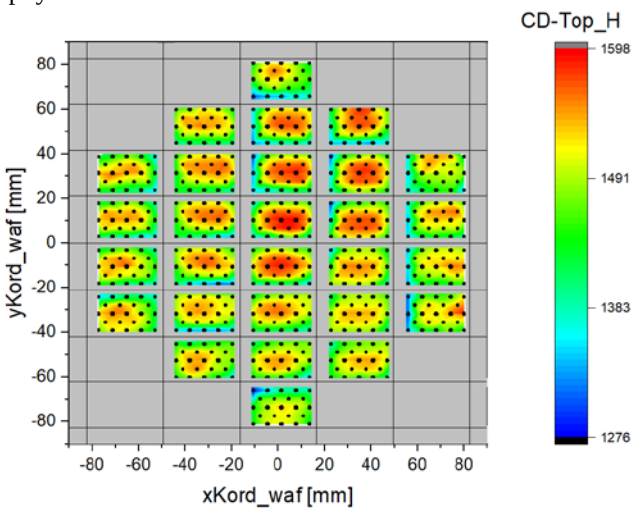


Figure 7: Wafermap for visualization of the slit width distribution across the wafer and chips as measured by CD-SEM. Black points indicate measurement positions.

In usual semiconductor processes there are two strategies to improve the CD uniformity. The first is the implementation of filling structures like passive mirrors around the active pixel area. However depending on the device specifications

and intended use, it might be forbidden to implement such structures due to the undesired scattered light from such fill pattern. The second option would be the application of optical proximity correction (OPC). By adjusting the slit width on the mask one could increase in the outer pixel area and decrease in the inner pixel area in an opposite way to compensate for this effect. The use of OPC is well established, however fails here, because of the chip stitching. Since the pixel area is patterned by exposing multiple times the same mask partition there is no well-defined outer and inner position of the pixel area on the mask. Another way of improvement of the CD uniformity is the separation of the litho-etch sequence into two different steps as demonstrated in Figure 8. In this process flow the first resist mask defines the mirror slits only, in contrast to the standard process, and fully covers the periphery (1). For etching there are now two areas (2), the pixel area with an open area of ~3% and the periphery with 0%. The absolute difference here is negligible compared to the standard process. In a second sequence, the pixel area is covered completely with resist, while the periphery is free of resist (3). The large difference in open area in this step (0% pixel area vs. 100% periphery) is of no relevance since there are no structures of critical dimension in the periphery. Furtheron, the thickness of the underlying sacrificial layer is of appropriate thickness so that local variations of the etch rate will not damage any underlaying structures. After etching, the result is the same like with the standard process (4) but without the CD variation of the one-step etch process.

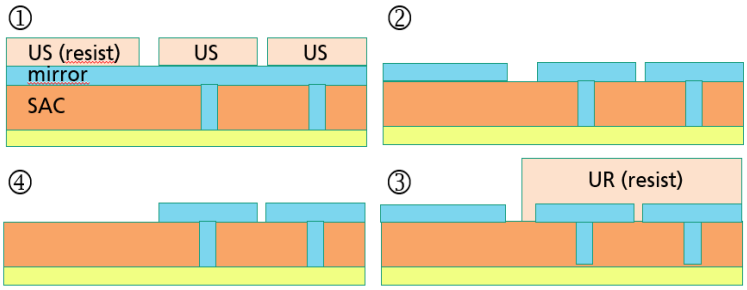


Figure 8: Process flow for the optimized process using two subsequent litho/etch sequences for mirror patterning. 1: After first lithography covering the periphery area. 2: After RIE patterning the mirror slits only. 3: After second lithography, covering the pixel area. 4: After second RIE, removing the mirror material in the periphery.

Figure 9 shows the mirror slit width distribution using the two-step sequence. The full CD-range is reduced from ~330nm to ~90nm. Especially in the wafer center there is no systematic CD-variation present anymore. Only at the wafer edge a systematic effect is visible. However, the absolute value still is much smaller than for the standard process. It is likely that such a non-uniformity is an effect caused by an inhomogeneity of the resist spin-coating or a non-ideal performance of the single-zone hot plate since such an effect is observed for other layers with more equally distributed open area values too. Although the introduction of one additional litho-etch sequence into the process flow has a negative impact regarding cost and manufacturing time, the gain in CD-uniformity by at least factor of 3.5 has a significant impact on the device performance and thus leads to a higher chip yield. The benefit of this two-step process therefore clearly exceeds the drawbacks.

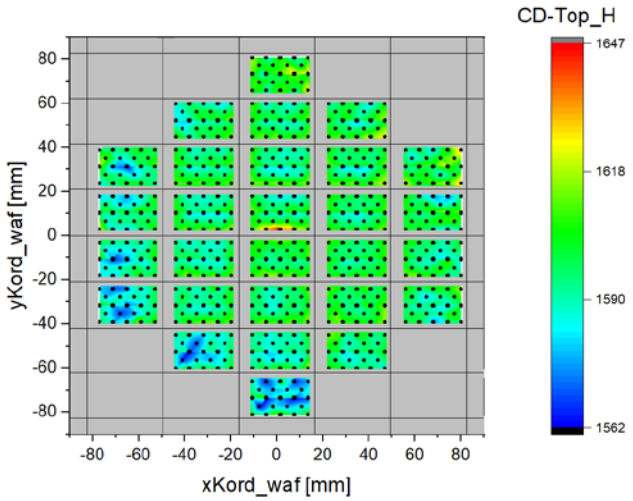


Figure 9: Wafermap for visualization of the slit width distribution across the wafer and chips as measured by CD-SEM. Black points indicate the measurement positions.

2.6 Pattern Fidelity

IPMS offers a wide range of different MMAs, especially regarding pixel number and pitch. The possible torsion of a hinge and thus the deflection angle θ of the mirror depends on the hinge dimension in the following manner:

$$\theta \sim l/wt^3 \qquad (1)$$

Here, l denotes the hinge length, w is the hinge width and t is the hinge thickness. To obtain reasonable deflection angles either the hinge length should increase or thickness and width should decrease. In the IPMS product portfolio, there are MMA with smallest pixel sizes down to 4x4µm, designed for future application such as holography [14]. The pixel size P however limits the hinge length by $l \leq P/2$ for orthogonal direction or $l \leq P/\sqrt{2}$ for diagonal direction. In addition, the minimum hinge thickness the most sensitive parameter for torsion, is limited. Common materials for hinges are Si or SiGe deposited by CVD or Al or TiAl deposited by sputtering. Both deposition techniques have their shortcomings for ultra-thin films especially if high uniformity is required. Other techniques that are more suited for ultra-thin films like atomic layer deposition (ALD) or molecular beam epitaxy (MBE) are often not available for the mentioned materials, especially in a semiconductor manufacturing clean room. The IPMS uses TiAl hinges down to 20nm thickness with $3\sigma \leq 0.5nm$. For sufficiently high drive sensitivity this might lead to the consequence, that one must reduce the designed hinge widths to a level of the resolution of the applied lithography level, e.g. 350nm for the NSR-2205i14E2 i-Line stepper currently used at IPMS. In some of our MMA-technologies the electrical force is applied between an electrode and the mirror [2], while for others they act between an electrode and a yoke, patterned in the same layer as the hinge [15]. While in the first scenario the hinge itself can often be designed as a quasi-isolated line, the structures in the second scenario become denser or like a line-space pattern. Dense structures are more critical regarding the resolution limit of the used lithography technology and therefore suffer from insufficient pattern fidelity. However, they are often necessary or at least beneficial regarding the applicable deflection angles since the effective actuator gap is smaller than for the first scenario. Figure 10 shows a typical structure of the yoke-type. One can see the typical optical proximity effect (OPE) at the outer edges of the yoke as well as at the connections hinge – yoke and hinge – post. In the first one the OPE could just decrease the effective area of the yoke, which has a small and usually not measureable effect on the drive sensitivity. The second one is more crucial since it decreases the effective hinge dimensions compared to design. Depending on the designed dimensions and the impact of the OPE, this effect could also change the effective hinge width (e.g. CD). This happens when the edges of the hinges inside the region of interest (ROI) of the CD-SEM measurement are heavily disturbed to a concave shape instead of a parallel pair of lines. In such case, one can configure the algorithm for the CD-SEM to measure only the minimum value at the narrowest position instead of fitting the best possible straight line to each edge. The effective or averaged hinge width, however, is higher than this minimum value and often even higher than the designed width. Regarding to Equation (1), a decreased length and an increased hinge width leads to smaller possible deflection angles of the mirror. If one cannot compensate this by higher voltages, e.g. due to limitations of the

CMOS, this will prevent an optimal operation of the MMA device. To avoid or minimize the OPE, optical proximity correction (OPC) is commonly used. In a structure like the one shown in Figure 10 notches at the connection points of the hinges are preferable to reduce the visible corner rounding. To show a perceptible effect, such OPC structure must have an appropriate size, which might be prohibited by existing design rules. To overcome the OPE issue for better pattern fidelity as well as to shrink future feature and pixel size, advanced lithography tools, i.e. in form of 248nm DUV lithography is recommended as described in Section 3.

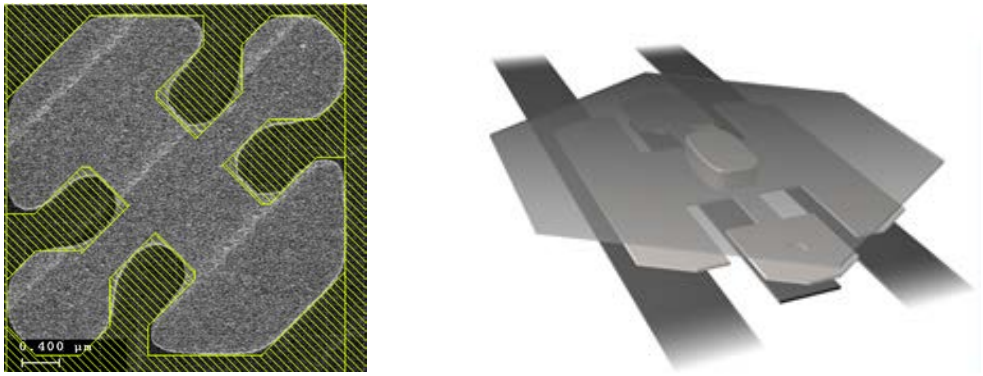


Figure 10: (left) Insufficient 2D-Pattern fidelity using i-Line lithography, CD-SEM image of a hinge/yoke structure in gray-scale. Overlay in lime: the original design on the mask. (right) Position of the hinge/yoke structure in a MEMS micro-mirror device [15].

3. OUTLOOK

3.1 DUV Lithography

Facing the increasing requirements for future MEMS devices regarding CD, OVL and pattern fidelity, Fraunhofer IPMS has invested in advanced lithography equipment. This could be realized only with exceptional European / National funding as part of the FMD project [16]. The Research Fab Microelectronics Germany (FMD) is a cross-site cooperation of eleven institutes within the Fraunhofer Group for Microelectronics together with the two Leibniz institutes FBH and IHP. Together they offer a One-Stop-Shop for technologies and systems in micro and nanoelectronics along the complete value chain.

A NIKON NSR210D DUV (KrF) Scanner clustered with a TEL CLEANTRACK ACT8 for patterning of subcritical layers (<400nm) with superior overlay performance ($\leq$9 nm) offering excellent cost of ownership performance have been setup in our cleanroom only lately (Figure 11). This equipment will serve as a first-of-a kind DUV litho cell for 200mm MEMS-on-CMOS applications in FEoL environment. Currently, process setup and integration into the MEMS manufacturing flows are ongoing. Target will be to consecutively substitute critical i-Line litho layers of current and future MEMS devices with DUV litho in a suitable Mix&Match integration scheme to realize accurate patterning well below 400nm critical dimensions. A first application will be the implementation of SLM in the field of holography within the European project RealHolo.

Figure 11: Nikon NSR-S210D KrF Scanner clustered with TEL CLEANTRACK ACT8 currently setup at Fraunhofer IPMS (courtesy of NIKON / TEL)

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