REALHOLO

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realholo.eu

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Developing Real World Technologies for Mixed Reality Worlds

Phase modulating micro mirror array for real holographic mixed-reality displays

Message from the Coordination Team

REALHOLO paves the way for mainstream mixed reality environments by using micro mirror arrays to provide the best possible experience for the user. The required natural visual experience can only be achieved with real holographic displays. In the past months the REALHOLO project made a big step forward with the research and development of a new type of SLM, a micro-electro-mechanical system (MEMS) based reflective micro-display: a micro mirror array (MMA) component with a unique set of properties. This was impressively shown at the first face-to-face meeting in Dresden beginning of October 2022. The consortium met at Fraunhofer IPMS and SeeReal and got some demonstrations on the latest results. Further, the meeting was dedicated to discussing the progress over the past months, the status and main achievements as well as an overview of ongoing and planned activities of all work packages. In the third edition of the REALHOLO newsletter we focus on the project status (mainly WP2 and WP3) and the next steps. For more detailed information about the project, we invite you to visit our project website, which is constantly updated with the latest project related news: www.realholo.eu.

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Budget

€ 6 Million
100% EU-funded

Consortium

8 Partners
6 countries

Duration

48 Months
01/2021 - 12/2024

The REALHOLO Consortium

The REALHOLO consortium consists of eight partners from six different countries:

Technikon Forschungs- und Planungs-gesellschaft mbH, Austria

OmniChip Sp. z o.o., Poland

Fraunhofer – Institute for Photonic Microsystems, Germany

nSilition SRL, Belgium

Sencio BV, Netherlands

SeeReal Technologies GmbH, Germany

Valeo, France

X-FAB Silicon Foundries SE, France

More information about the consortium can be found on the project website:

https://realholo.eu/partners/

REALHOLO project status and next steps

In the past months the consortium focused mainly on WP2 and WP3. The backplane and driving electronics development is a major milestone in the project. Also, the MEMS process and MMA component development is of paramount importance.

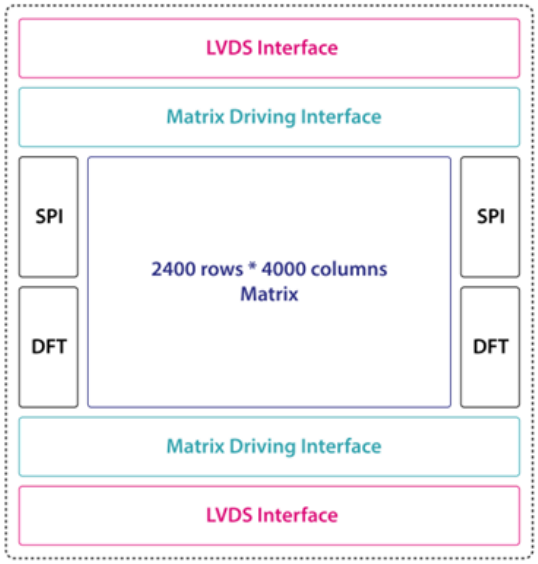
Completed and ongoing activities in WP2 - Backplane and driving electronics development

The design of the CMOS backplane integrated circuit is pursued with the completion of the design and layout of the functional blocks. The design and the layout of the LVDS receiver, the de-serializer and the clock/data tree is completed and verified for layout parasitic effects. The transfer (from another fabrication process) and the redesign of all the functional blocks necessary for the elaboration of all the companion cells of the library has been executed. In parallel, the design of the analog column drivers, including the DACs is executed. Along with the progression of the integration, the higher level of the architecture of the chip could be confirmed. The top-level integration of the chip is now progressing and top level simulations are starting up.

The preparation for the experimental test chip analysis has been done with clear documentation of all experiments and test pattern generation including Cell-Aware Test with relevant fault rules files and Stuck-At patterns so that the benefit of new test methodology can be assessed.

To summarize, the following achievements and results are reached in WP2:

- The design and the layout of the LVDS receiver, the deserializer and the clock/data tree is completed.
- The design and the layout of the DACs and the column drivers is completed.
- The row driver has been designed and layouted. It is tested with the complete pixel matrix.
- The higher than expected leakage current of the pixel has been lowered and the effects have been reduced back to the acceptable limits.
- The specification of the digital decoder is done. A first draft implementation has been completed. A draft layout has been edited.
- A first top level schematic has been edited.
- Top level simulations have started.



Completed and ongoing activities in WP3 - MEMS process and MMA component development

In WP3 the development of the MEMS manufacturing process has been continued and has reached the point where working versions for almost all necessary process steps and modules are available and tested in the more challenging version for smaller feature sizes using DUV lithography. Nevertheless, the development is continued for improvements.

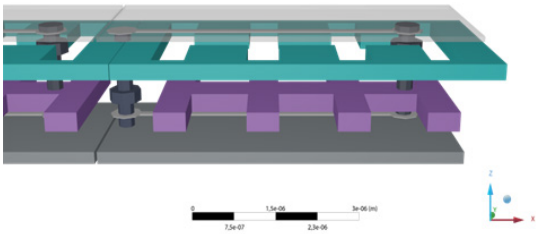
While the first full wafer run of passive MMAs suffered from various manufacturing errors, the second lot has been completed by end of August 2022 and first chips are packaged to be characterized.

An improved actuator design enabled by DUV lithography offers almost zero crosstalk without negative side effects.

The packaging development has been progressing. A first phase of the design and simulation of the packaging substrate has been done with promising results.

For the precision alignment of the beam combiner on the MMA chip tests have been planned and dummy material and tools have been designed, ordered and are available at IPMS. Actual test runs are about to start.

Extensive FEM simulations show the behaviour of the package over the full operating temperature range. Here the results are not fully satisfying the requirements, yet, but plans for further investigations have been set up.



To summarize, the following achievements and results are reached in WP3:

- The MEMS manufacturing steps and modules have been developed in a first version optimized for DUV lithography.
- Processing steps and modules are now tested and available for almost the complete manufacturing cycle.
- The first wafer lot of small passive SLM chips is finished - characterization is about to start.
- The manufacturing of wafer lots of full-sized passive SLM chips is proceeding.
- The spring layers can now be manufactured with smaller feature size and better precision using DUV lithography.
- A shield ring has been developed that suppresses crosstalk between neighbor pixels almost completely in simulations.
- The design and simulation work of the packaging substrate shows promising results.
- Extensive FEM simulations show the behavior of the package over the full operating temperature range.
- Dummy material and tools for alignment tests of the beam combiner on the MMA chip are available, test runs about to start.

There still is a variety of steps and activities planned for the next project phases to implement the full scope of the REALHOLO project in order to achieve the expected revolutionary impact for our society.

Submitted deliverables of WP2 and WP3:

D2.1 "CMOS backplane subcircuit design and use of CMOS test chips"

D2.1 "CMOS backplane subcircuit design and use of CMOS test chips" unveils the technology used to convert the digital representation of the hologram computed by a 3D image processor into a plurality of voltage stimuli that deflect each individual pixel of the matrix of mirrors. The stroke of the mirror is controlled by the voltage stimulus, which then, when illuminating the SLM, will be used for holographic image generation. The black-plane chip is generating these voltages from digital input data in the REALHOLO system and can be seen as a gigantic very high-speed digital to analog converter (DAC).

D2.3 "Report on results for reliable digital IPs and their compliance to automotive standards"

D2.3 "Report on results for reliable digital IPs and their compliance to automotive standards" focus on the digital part design with the foundation IP as digital library containing set of standard cells. For that, a so-called zero-DPPM (zero Defective Part Per Million) digital library have been developed. The objective to reach a very low failure rate in the field is extremely important for the REALHOLO CMOS back-plane IC since some applications are finding place in the automotive market.

D3.1 "Report on MEMS process and actuator design development" and D3.2 "Report on MEMS development"

D3.1 "Report on MEMS process and actuator design development" and D3.2 "Report on MEMS development" document the progress and status of the MMA development. The deliverables report on the MEMS manufacturing process development as well as the refinement of the actuator concept, the prediction of the actuator properties, and the determination of suitable manufacturing parameters like thicknesses of structural and sacrificial layers and design details.

D3.3 "Report on the package design"

D3.3 "Report on the package design" reports on the package for the holographic 3D display in REALHOLO that protects the sensitive MEMS die from mechanical and chemical harm in the environment whilst maintaining optical access to the micro-mirror array. During the coming months, the packaging options will be optimized and the requirements of placement accuracy and SLM bow change will be traded-off and re-assessed against the background of the work on the HUD design.

See all public deliverables:
https://realholo.eu/public-deliverables/

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This project is an initiative of the Photonics Public Private Partnership.

Upcoming Events

SPIE OPTO conference 2023 (Photonics West)

January 28 - February 02, 2023

@ San Francisco, USA

Industry (Advisory) Board Meeting

March 29, 2023

Past Events

SPIE Photonics West 2022

January 22-27, 2022

@San Francisco, USA

Digital Holography and Three-Dimensional Imaging - OPTICA (formerly OSA)

August 01-04, 2022

@ Cambridge, UK

First face-to-face Technical Meeting

October 05-06, 2022

@ Dresden, Germany