AUTHOR INTRO DR. CHRISTOPH HOHLE

- Christoph Hohle received his Ph.D. degree in 2000 from the University of Bayreuth, Germany, Macromolecular Chemistry Department, where he was working in the field of photorefractive polymethacrylates and amorphous low molecular weight glasses. He joined Infineon Technologies' Memory Product Division (later Qimonda) in 2000 where he originally focussed on design and synthesis of 157nm and 193nm photoresists for optical lithography. In 2004 Dr. Hohle joined the Center of Competence E-Beam at Qimonda Dresden, working as Staff Engineer responsible for the resist process. From 2009, he led the NanoPatterning / E-Beam Litho Group at Fraunhofer Institute for Photonic Microsystems (IPMS) in Dresden. Since 2016 he is team manager for technology development at the IPMS' Business Unit Spatial Light Modulators.
- Dr. Hohle has been active with SPIE Advanced Lithography for many years as Chair & Co-Chair of the Advances in Patterning Materials & Processes Conference. He has (co) authored more than 75 papers and numerous patents in the field of photolithography.

Fraunhofer IPMS

SPIE. PHOTONICS WEST

Challenges of monolithic MEMS-on-CMOS integration for spatial light modulators

SPIE Photonics West -- OPTO2021 -- San Francisco / USA & Online

MOEMS and Miniaturized Systems XX Conference 06. – 11.3.2021

Session 7 - Imaging

Paper 11697-29

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CONTENT

- Short Intro Fraunhofer IPMS
- MEMS-on-CMOS Concept
- Surface MEMS Technologies for SLMs
- Challenges and Solutions for MEMS-on-CMOS Integration
- Summary and Outlook

FRAUNHOFER GESELLSCHAFT

APPLIED RESEARCH TO BENEFIT SOCIETY

- Industry
- Service
- Public

THE EUROPEAN INNOVATION POWERHOUSE

- 72 Institutes (in Germany)
- 26.600 employees
- 2.6 Mrd. € turnover (research)

IDEAS TO MARKET

- Professional IP-management
- Leading edge equipment
- From sketch to products

IPMS CLEANROOM FACILITIES

200 mm MOEMS/MEMS clean room

- 1500 m², class 10 (ISO 4)
- 200 mm / 8“ wafer size
- 3 shift operation (24/5) for R&D and pilot fabrication
- Technological parameter supervising system (MES)
- PPS based planning and documentation
- ISO 9001 certification

300 mm clean room (BEoL, CNT)

- 4000 m² clean room, class 1000 & 200 m² laboratory area
- 80 Tools for Wafer Processing, Patterning, Metrology & Analytics
- Qualification of processes & materials on 300 mm industrial standard equipment
- Sub-nm characterization and verification
- Full integration into customer process flow in 28 nm technology and beyond

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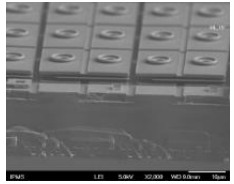
WHY MEMS-ON-CMOS?

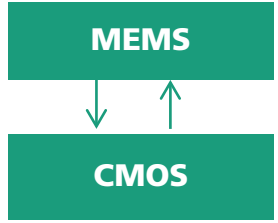
MEMS – Micro- Electro- Mechanical Systems to ***sense*** or ***control***

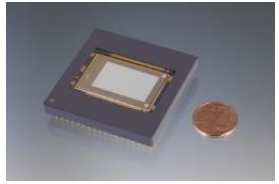
physical quantities | **chemical quantities** | **optical quantities** | **biological quantities**

- ASIC/ CMOS – electrical interface for MEMS to outside world for
  - Communication
  - Amplification
  - Driving actuators
  - Signal conversion
  - Analog-to-digital conversion
  - Temperature compensation
  - Storage

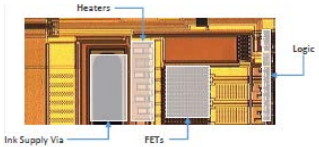


Micro-Bolometers

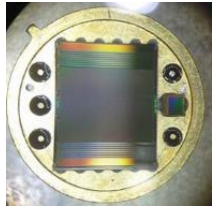




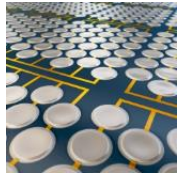
Micro-Mirror Array



Microfluidic Chips



Thermopile Arrays



CMUT Arrays

MEMS-ON-CMOS – MULTI-CHIP HETEROGENEOUS INTEGRATION

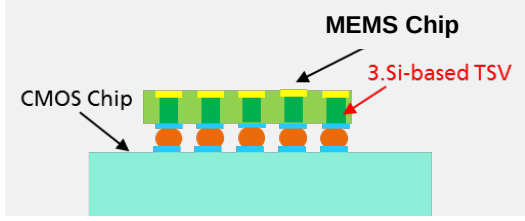
Merging on Chip-Level

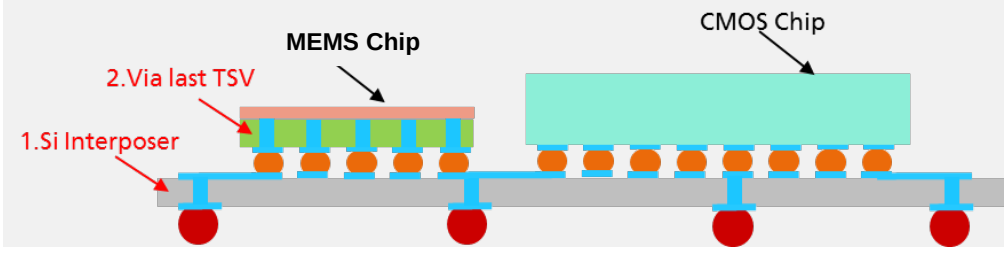
- Parallel fabrication of CMOS / ASICs and MEMS
- MEMS and CMOS designed, manufactured and tested independently
- MEMS manufacturing allows non-CMOS compatible processes (gold, copper, PZT)
- MEMS and CMOS connected via interposer using TSV technologies, ball grid arrays, flip-chip or wire bonding

Combination of specific MEMS with commercially available standard ASIC

→ simple, rapid and cost-efficient implementation

→ Limited integration density





MEMS-ON-CMOS – MULTI-WAFER HETEROGENEOUS INTEGRATION

Merging via wafer bonding – multi-wafer approach

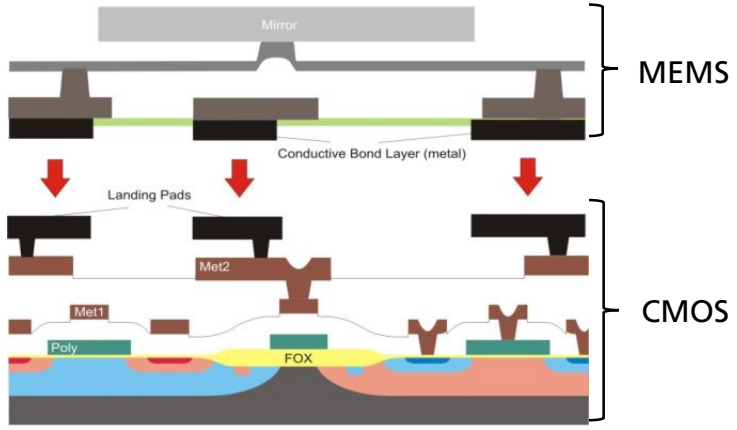
- MEMS and CMOS/ASIC will be pre-fabricated on separate substrates
- Via formation during layer transfer (via-first) or after layer transfer (via-last)
  → for establishing mechanical and/ or electrical contacts
- Via-first approach using metallic bond between two metal layers on separate wafers (e.g. Al/Ge eutectic bond or Cu thermo-compressive bond)
- Via-last approach integrates contacts after bonding

Advantage:

Integration of high performance materials (c-Si) and high temperature processes for MEMS wafers

Drawback:

High alignment accuracy necessary, integration density limited and bond yield is still a critical issue



MEMS-ON-CMOS – MONOLITHIC INTEGRATION

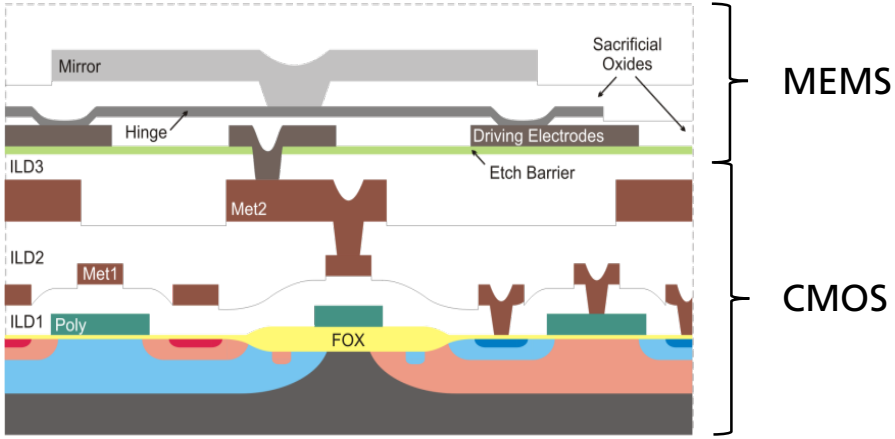
- Can be performed as MEMS-first, interleaved and **MEMS-last integration**
- Applying bulk or surface micromachining after completion of CMOS/ IC
  - Interconnection are realized using standard CMOS processes
    → very reliable and high integration density
  - Substrate temperature during MEMS processing is limited to 450°C
  - Integration in existing CMOS line or specialized MEMS Fabs

Advantage:

Realization of rather complex MEMS
→ MEMS/ MOEMS arrays

Drawback:

450°C max. process temperature
material limitation



MEMS-ON-CMOS – CONCEPT

- Use of foundry fabricated CMOS backplanes
  - High flexibility regarding CMOS nodes and PDKs on 200 mm wafer size
  - Shorten time-to-market for our customers by:
    Separating MEMS from CMOS development and processing
    Final implementation of MEMS on external CMOS wafers
- **IPMS is focused on monolithic MEMS integration on CMOS**

  High integration density
  ➢ Smaller system dimensions, lower power
  ➢ Less parasitic effects

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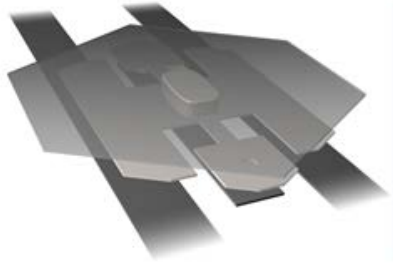
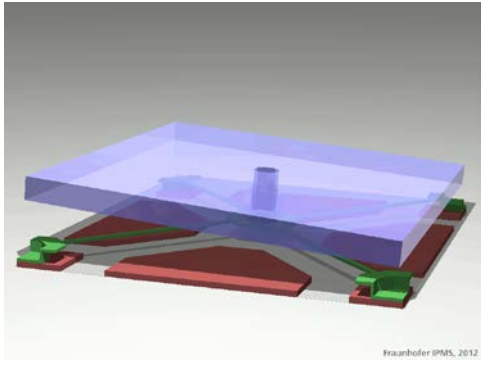
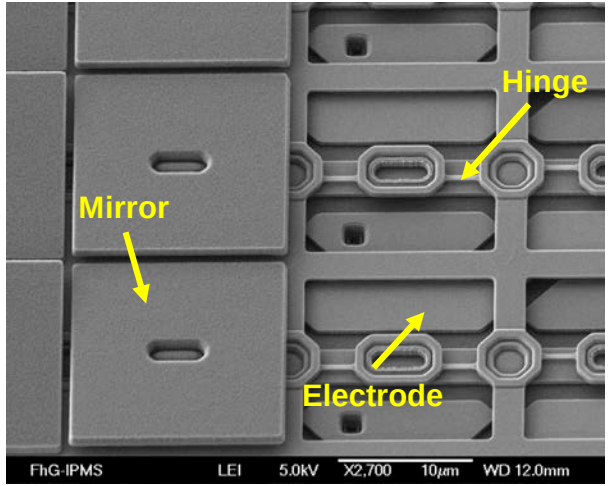
SURFACE MEMS TECHNOLOGY - SPATIAL LIGHT MODULATORS

- Characteristics of SLMs
  - Analog deflection
  - UV/DUV application (248 / 193nm)
  - Planarity / bow < 5 nm @ 16 µm mirror pitch
- 2nd Generation Spatial Light Modulators
  - Multi-level architecture with separation of mechanical parts from mirrors
    - Actuator/ hinges: amorphous materials
    - Mirror: Al-Alloy
  - Inorganic sacrificial layers
- Integration of high reflectance mirrors
  - Multilayer design for UV-VIS-NIR
  - Using hybrid multilayer stacks to reach sophisticated reflection



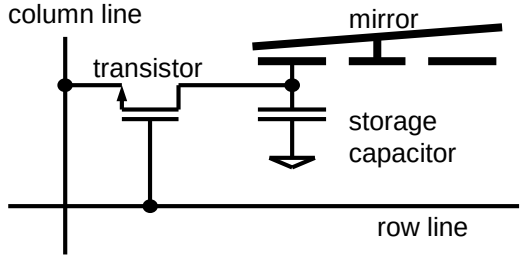




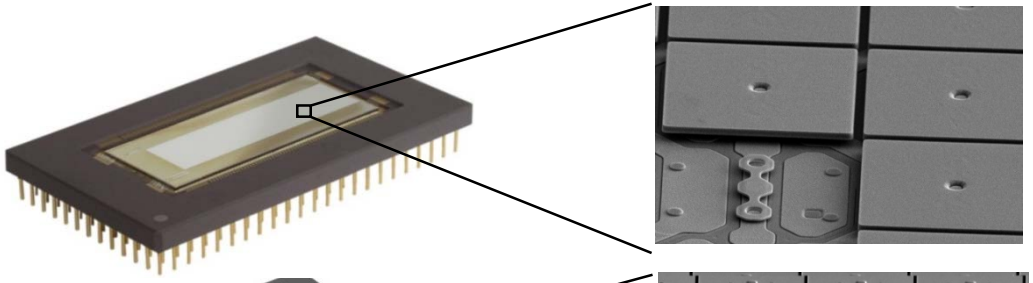
SURFACE MEMS TECHNOLOGY - SPATIAL LIGHT MODULATOR

Application & customer specific micro mirror device development and optimization

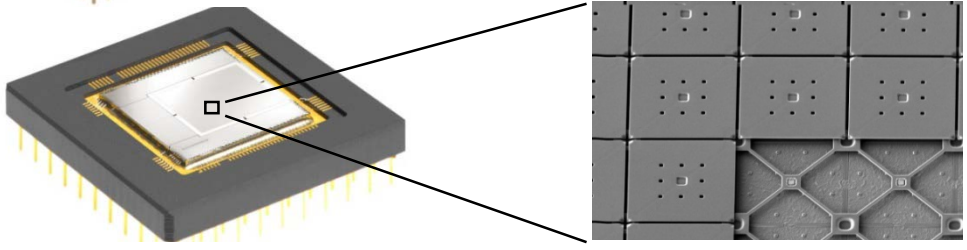
Device examples with analog deflection control:



- 2048 x 512 tilt mirror array
  for sub-µ lithography
  16 µm pixel size



- 240 x 200 piston mirror array
  for optical phase control
  40 µm pixel size



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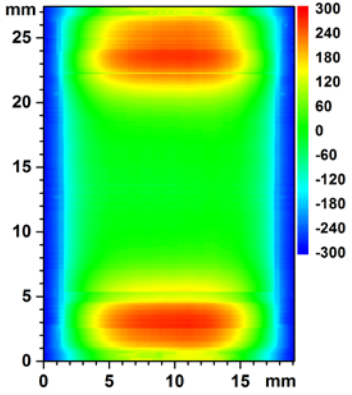
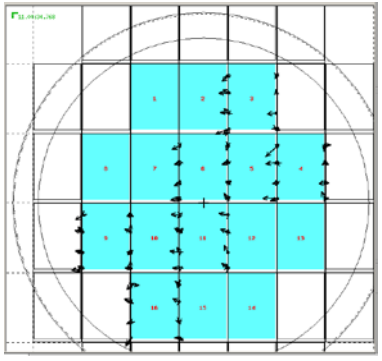
MEMS-ON-CMOS: IPMS CONTROLS INTERFACE TO CMOS FAB

- Tuning surface planarity after CMOS manufacturing
- Mix-and-Match Lithography between fab and IPMS
- Additional chip edge protection in case of surface MEMS
- High accuracy for large optical chips
- Special contamination handling for backplanes containing Cu

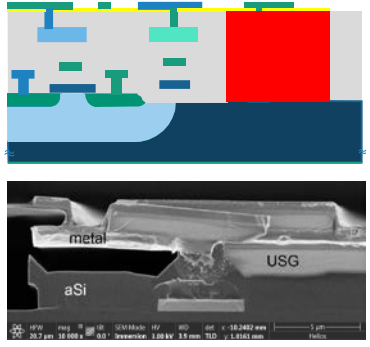
Surface Planarity CMOS Backplane



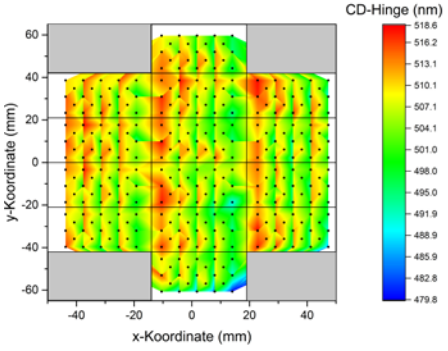
Mix-and-Match Lithography



Additional Chip Edge Protection against HF



Adapted Stitching for large optical chips

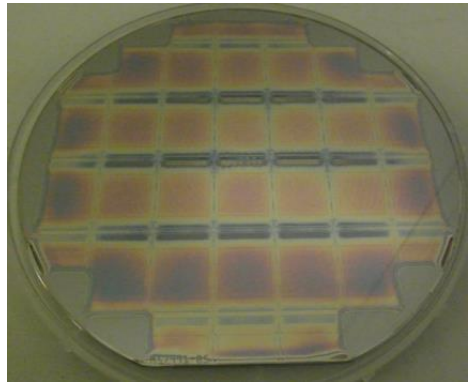


SPIE. PHOTONICS WEST

Fraunhofer IPMS

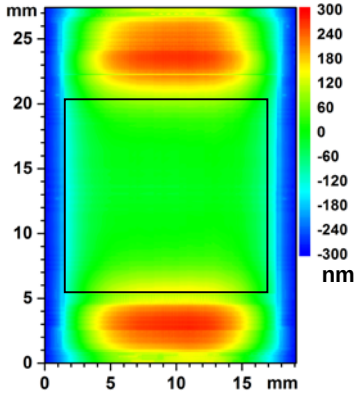
CHIP TOPOLOGY – OPTIMIZATION

- High surface inhomogeneity after CMOS processing due to interconnection pattern / fill factors are visible
- Hight difference between areas can be leveled-out using CMP
- Results are **not satisfying** with CMP only



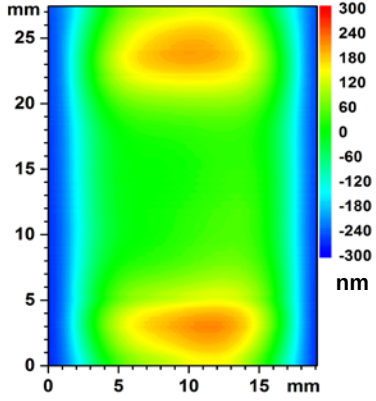
Initial state

after fab



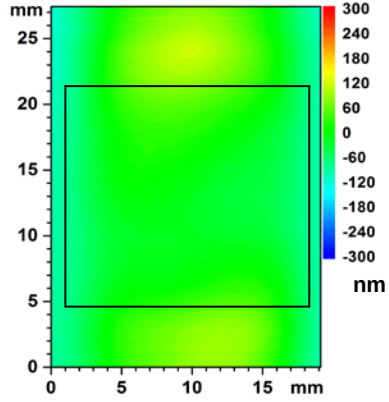
+200 nm SiO_2

+ CMP



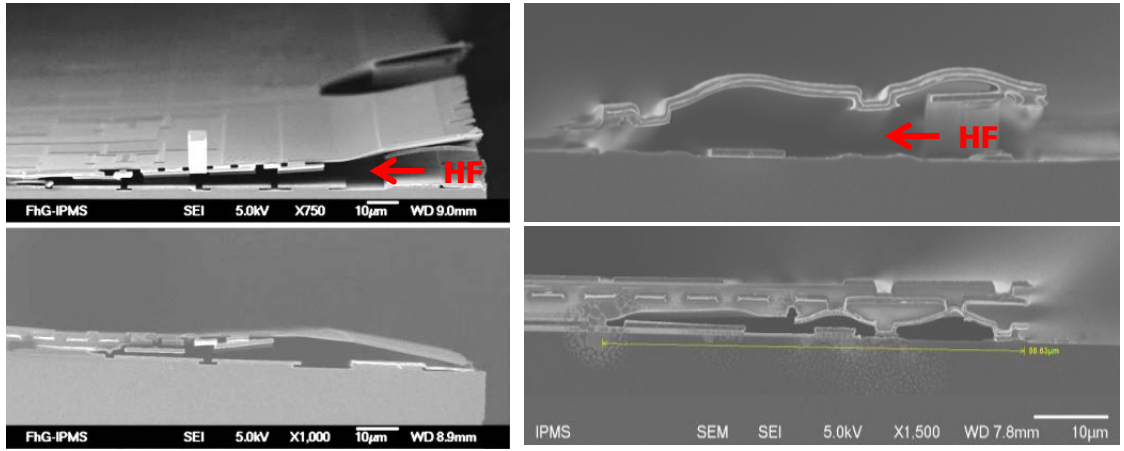
+700 nm SiO2

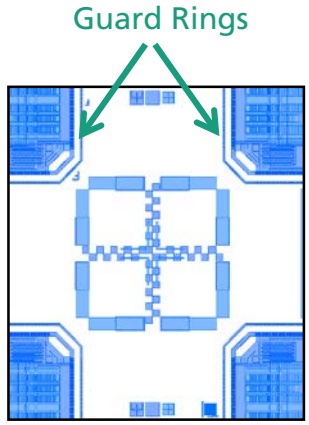
-500 nm inverse etching

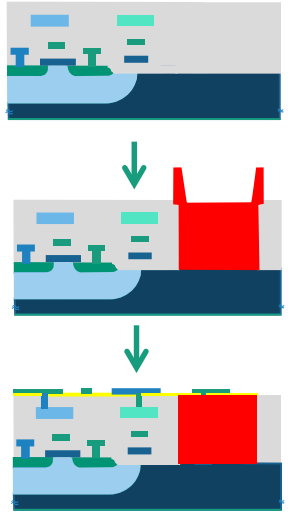


CMOS BACKPLANES AND SACRIFICIAL LAYER TECHNOLOGY

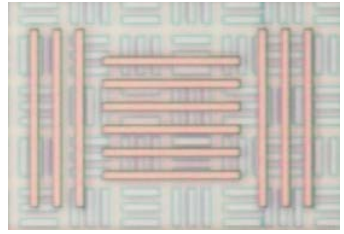
- Using sacrificial layer technology based on SiO_2 for MEMS actuators
  - HF release on chip level after dicing
    - Large variety of MEMS chips can not be diced after HF release
    - Doped oxides (e.g. BPSG) show higher HF etch speed which leads to massive undercut on edges
    - Chip edges need protection
  - Guard rings (ESD protection, stacked contacts) may help to limit under-etch



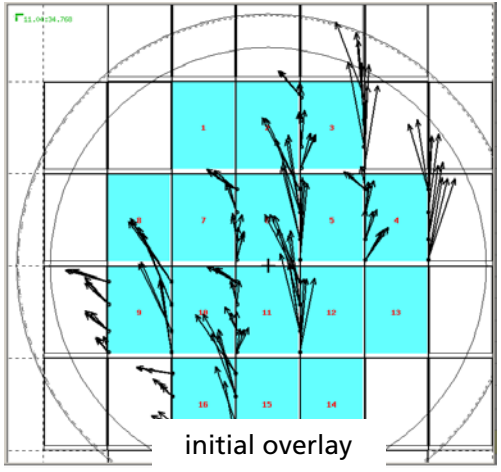




MIX & MATCH LITHOGRAPHY



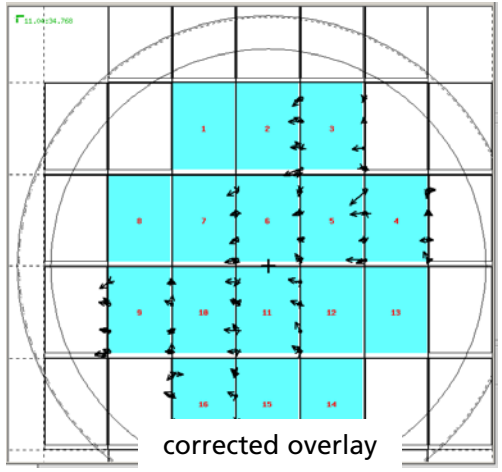
- Essential for MEMS-on-CMOS: perform an accurate Mix & Match lithography with high overlay accuracy BEoL → FEoL
- Using i-line lithography and overlay measurement in combination with litho rework → accuracy of ~50 nm (stepper specs)



initial overlay

Property	Unit	Min.	Mean.	Max.
OVL (X)	nm	-90,6	-22,0	56,1
OVL (Y)	nm	6,8	93,1	182,2

- Calculation of correction factors
- Rework
- Illumination with applied correction factors

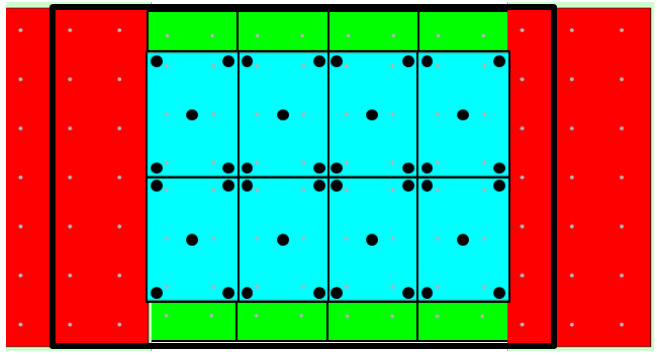


corrected overlay

Property	Unit	Min.	Mean.	Max.
OVL (X)	nm	-40,0	-4,0	24,0
OVL (Y)	nm	-31,1	-0,1	28,5

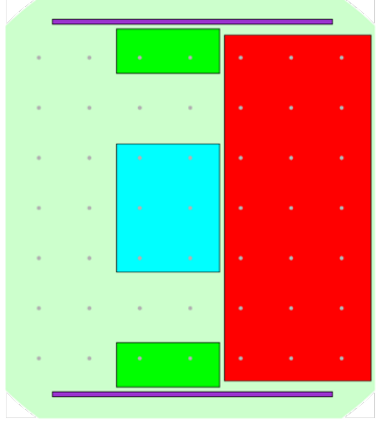
REALIZING LARGE CHIPS

- MEMS features may exceed maximum litho exposure field
  → e.g. IPMS fabricates chips larger than 26 x 33 mm²
- Need for complex litho stitching / partitioning



stitching chip

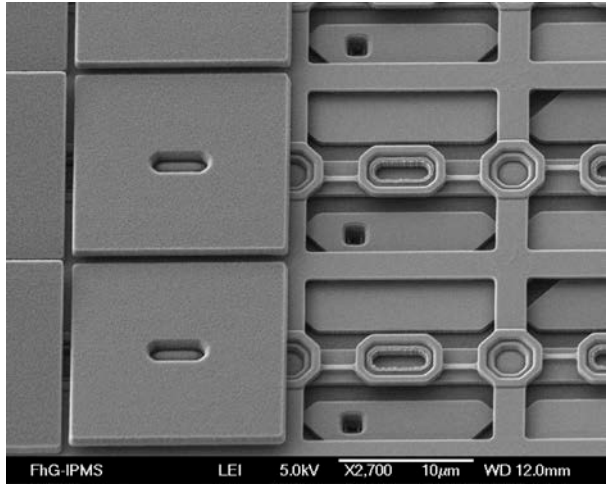
- Example: 72 shots / chip → ~1600 shots / 200 mm wafer ~ 40 min/wafer
- Balance exposure time versus exposure accuracy to avoid drift effects and to achieve very good CD/OVL values
- Adapt and control design features to minimize stitching effects

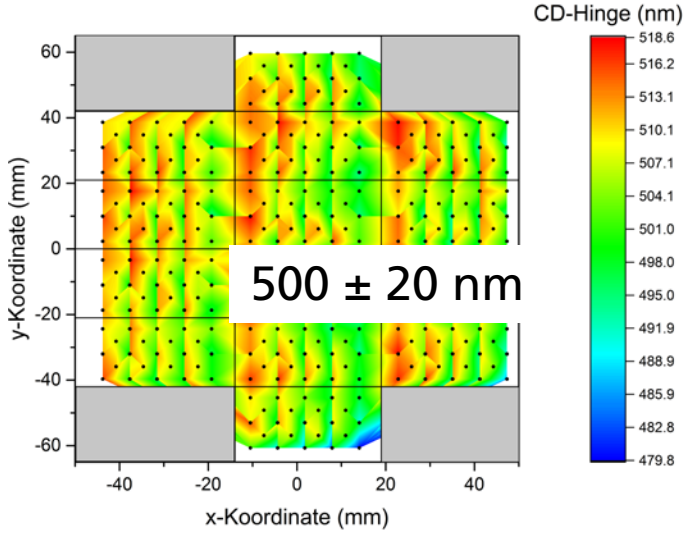


reticle layout

PROCESS UNIFORMITY

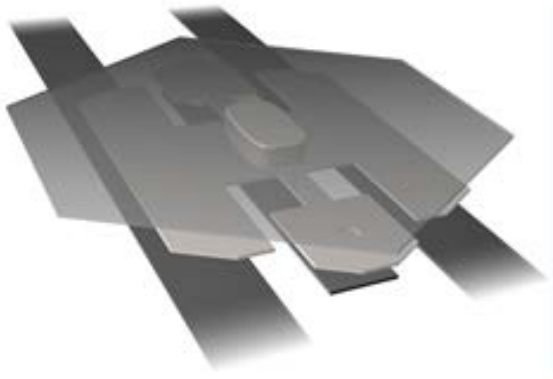
- Criticial litho features need tight process control (e.g. via CD-SEM)
  … e.g. mirror slits, hinges, holes, …
- Example:
  - hinge width with a target of 500 nm

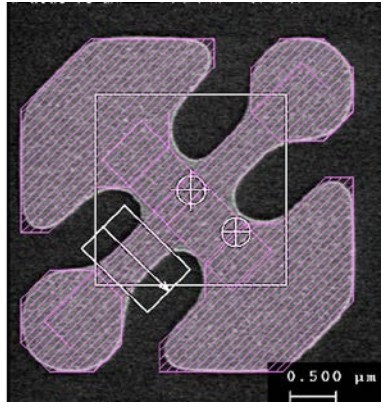




PATTERN FIDELITY

- Criticial MEMS features approaching resolution limit of currently used i-Line Litho
- Insufficient 2D-Pattern fidelity
- CD-SEM image of a hinge structure in gray-scale. Overlay in pink the original design on the mask. The white lines mark the pattern recognition box and region of interest (ROI) for CD-SEM measurement





DUV LITHOGRAPHY @ FRAUNHOFER IPMS

- First-of-a kind DUV litho cell for 200 mm MEMS-on-CMOS applications
- Installation in 12/2020, process setup ongoing
- Significant funding by EU / German government (FMD)

Forschungsfabrik Mikroelektronik Deutschland

NIKON NSR S210D

TEL CLEANTRACK ACT8

SUMMARY

- Monolithic MEMS-on-CMOS Integration offers a solution for a variety of complex optical and mechanical MEMS applications
- Control of interface to CMOS Fab (Foundry) essential
- Fraunhofer IPMS as leading edge supplier with broad MEMS-on-CMOS capabilities
- i-Line litho @ the limit to serve current process requirements
- The MEMS future is DUV ☺

ACKNOWLEDGEMENTS

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- Visit Fraunhofer IPMS @ SPIE Photonics West Digital Marketplace

THANK YOU FOR YOUR ATTENTION

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