REALHOLO

Developing Real World Technologies for Mixed Reality Worlds

Phase modulating micro mirror array for real holographic mixed-reality displays

Issue 04

January 2025

realholo.eu

@RealholoH

realholo-h2020

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Budget

€ 6 Million
100% EU-funded

Consortium

7 Partners
6 countries

Duration

60 Months
01/2021 - 12/2025

Message from the Coordinator

The REALHOLO project made significant progress in developing a novel MMA-based SLM (Spatial Light Modulator) and demonstrating its capabilities in a real holographic MR (Mixed Reality) application.

- The CMOS backplane design and the challenging packaging substrate design was verified through extensive simulations and finalized with high quality.
- Progress was made in MEMS manufacturing with steady improvements in MMA chip quality despite setbacks, with promising results and recent wafer lots yet to be characterized.
- The finalized actuator design now includes advanced features like a shield ring and optimized geometrical parameters.

Nevertheless, some significant amendments and updates within the REALHOLO project were ongoing. These modifications are crucial for adapting to unforeseen circumstances and ensuring the continued success of the project.

The ongoing automotive crisis has presented challenges that have impacted the REALHOLO project. Some operational challenges have necessitated a strategic decision to restructure the consortium. We welcome Holoeye and Realview Imaging into the consortium, introducing alternative use cases that align with the project's objectives. Additionally, Fraunhofer IPMS took on the role of the technical lead, ensuring continuity and expertise within the consortium.

The REALHOLO consortium consists of 7 partners from six different countries:

Technikon Forschungs- und Planungs-gesellschaft mbH, Austria

OmniChip Sp. z o.o., Poland

Fraunhofer – Institute for Photonic Microsystems, Germany

nSilition SRL, Belgium

Real View Imaging Ltd, Israel

HOLOEYE Photonics AG, Germany

X-FAB Silicon Foundries SE, France

More information about the consortium can be found on the project website:

https://realholo.eu/partners/

REALHOLO project status and next steps

WP2 status update

In the previous reporting period, the design and development of the REALHOLO backplane ASIC advanced significantly. The ASIC design was completed with all functional blocks and analog column drivers, including DACs, verified for parasitic effects. The top-level integration was completed and simulations ran successfully. However, the available die size for placing and routing digital elements required reducing the number of pixels while still maintain [a SLM with] over 8 Megapixels. FPGA and evaluation boards were selected, and discussions on test setup architecture and validation began. Efforts also focused on reducing defects in the digital library and improving defect detection using cell-aware test patterns. Technical support for the LGA chip package substrate design was provided, reviewing the layout and recommending improvements to reduce signal interference and supply degradation. Simulations were conducted and electrical issues like supply line ringing were identified and resolved, resulting in an approved package layout. Work on the parametric validation setup for the backplane ASIC was performed, developing customized solutions, including a test board and FPGA code, to avoid using expensive and over-sized FPGA, off-the-shelf components and connectors. The parametric validation setup should create the best possible signal and power supply quality for the ASIC. Hence it should be kept simple and avoid the presence of connectors in the LVDS signal paths. On the side of the system-level evaluation board, the number of components can also be kept reasonable since there is no need to cover all the parametric test scenarios anymore. It also helps at keeping the complexity of the system-level evaluation board reasonable.

Key Highlights:

- Identified and resolved oscillation issues in the backplane ASIC substrate, improving performance and quality. New layout with simulated parasitic elements accepted.
- Designed differential probes for jitter measurements on a "dummy SLM." Best design selected based on results.
- Defined minimum impedance requirements for sub-matrix supplies to optimize decoupling capacitor placement, value, and positioning.
- Transferred backplane-only wafers for packaging and electrical testing.
- Work on derisking (by test boards and/or simulations) and preparation of the parametric test board and the system-level board while the package of the ASIC is still at design or manufacturing.

WP3 status update

Significant progress was made in processing wafers and chips for both passive (PHS) and active (AHS) devices. Transitioning to DUV lithography has improved pattern fidelity and layer overlay, though challenges such as deformed hinges and residuals from sacrificial layers occurred. Extensive characterization of PHS chips has yielded valuable insights, aligning closely with simulations and providing critical data on actuator parameters, and chip performance. Improvements to the MEMS manufacturing process are already showing promising results in recent PHS lots, and further enhancements are expected to benefit AHS devices.

Further, the characterization setup was advanced, automating measurement data analysis and confirming good results for parameters like mirror tilt, roughness, and flatness. Initial heat treatment tests have shown no measurable drift or deformation. Manufacturing latest PHS and the first AHS wafers has been completed, with characterization of these new lots imminent.

The packaging design, validated through extensive simulations, is finalized, and substrate fabrication is in progress. Preparations are underway to package AHS backplane chips (without MEMS) for electrical testing, with further work nearing completion for packaging AHS chips with MEMS mirrors. Despite challenges and delays, these advancements position the project for continued success.

Key Highlights:

- First wafers with MEMS mirrors on active backplanes are complete.
- Characterization setups and automated routines for measuring pixel response curves have been developed, achieving desired stroke and low nonlinearity.
- Process improvements have steadily increased the actuator quality.
- The packaging substrate design is finalized, verified via simulations, and fabrication is in progress.
- Packaging process development for AHS chips (with and without MEMS) is nearly complete.

WP4 - Amendment of Use Case: Augmented Reality for Medical In-Field Imaging

The project introduces an alternative use case focused on 3D Augmented Reality for medical imaging. This use case leverages Micro Mirror Array (MMA) technology to address the specific requirements of medical imaging, ensuring high image quality, low latency, and reduced crosstalk.

WP5 - Amendment of Use Case: Structured Illumination

A new use case focused on Structured Illumination is introduced, which is a very representative and popular use of phase-modulation for enhancing 3D capture, manipulation and measurement. Integration of MMA technology is expected to improve speed and accuracy for more complex pattern designs.

Extension of the Project

Delays in the design of the CMOS backplane ASIC and the MEMS manufacturing process necessitate an extension of the project timeline by 12 months. Mitigation actions have been applied to overcome challenges and ensure the successful completion of project objectives.

Papers Accepted at Conferences

Within the last year, REALHOLO submitted 7 papers to conferences that were accepted. This showcases the team's expertise and shares knowledge with the wider community:

Link to papers: **https://realholo.eu/results-downloads/**

- **MEMS-on-CMOS integration of a holographic 8M-Pixel SLM device using KrF-Lithography**
- **Characterization of MEMS piston mirror arrays with comb drive actuator**
- **Novel reflective SLM in real holographic 3D HUD displays and their impact on quality**
- **An FEM Study on Minimizing Electrostatic Cross Talk in a Comb Drive Micro Mirror Array**
- **Developing a Micro Mirror Array for Holographic 3D Displays**
- **First Characterization of Comb Drive Based Micro Mirror Arrays**
- **MEMS-on-CMOS-Integration of Spatial Light Modulator for Holographic MR/AR Applications**

Collaboration and Networking

REALHOLO has started cooperation activities with related projects, fostering a valuable network of professionals who support each other, exchange ideas, and potentially collaborate on future initiatives.

Correlation between REALHOLO and SPOTLIGHT:

A correlation call took place between REALHOLO and SPOTLIGHT, another Horizon Europe project funded under the same call. Although the projects diverged in terms of their primary focus, the call brought to light some synergy and potential for future collaborations. Please find more information about the SPOTLIGHT project on their website:

Spotlight – Sunlight production of chemical fuels

Correlation between REALHOLO and PHABULOuS:

REALHOLO and PHABULOuS Pilot Line started a project collaboration. We are excited about future collaborations, discussions and exchanging complimentary ideas to combine augmented reality and holographic experiences. REALHOLO partners join the PHABULOuS workshop on "Free-form Micro-Optics for consumer electronics" to discuss further collaborations. PHABULOuS is the one-stop-shop for free-form microoptics , taking designs and prototypes to large-scale manufacturing. Furthermore, they specialize in applications for AR and MR, utilizing the cutting-edge oled technology. For a glimpse into the diverse range of use cases, explore their website:

PHABULOuS – Pilot-line providing highly advanced & robust manufacturing technology for optical free-form micro-structures

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 101014977.

This project is an initiative of the Photonics Public Private Partnership.

Past Events

SPIE Photonics West 2023

January 28 - February 02, 2023

@San Francisco, USA

Technical and Industry Advisory Board Meeting

March 28-30, 2023

@ Cambridge, UK

CadenceLIVE Europe 2023

October 10-11, 2023

@ Munich, Germany

SPIE Photonics West 2024

January 30 - February 01, 2024

@ San Francisco, USA

SPIE Advanced Lithography + Patterning

February 25-29, 2024

@ San Jose, USA

Optogen 2024 - 9th International Workshop on Technologies for Optogenetics and Neurophotonics

April 15-17, 2024

@Prague, Czech Republic

FiO LS 2024 - Frontiers in Optics + Laser Science

September 23-26, 2024

@Denver, USA