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Dissemination report on MEMS results

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Abstract	This report lists the dissemination activities and successes regarding the MEMS development and integration, including a technical summary and a performance evaluation.
Keywords	MMA, MEMS, manufacturing process, actuator performance

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Disclaimer

Executive Summary

REALHOLO is a project to develop an advanced display system for real holographic 3D mixed reality (MR) applications, structured illumination, and other, related applications. The core component of such systems is a micro-mirror-based piston-type spatial light modulator (SLM) with challenging specifications, which has not been available before this project. REALHOLO is developing this new type of SLM based on micro-mirror-array (MMA) technology in its Work Package 3.

This document reports on the results of Work Package 3 of the REALHOLO project, which is structured into 4 topics.

The first of these topics, discussed in Chapter 2, is the actuator concept with reasons for our basic choices. It includes the prediction of the actuator properties by finite-element-simulations (FEM) promising superior actuator performance and the determination of suitable manufacturing parameters like thicknesses of structural and sacrificial layers and design details.

The second topic, discussed in Chapter 3, is the MEMS manufacturing process development. This is experimental work done in the Fraunhofer IPMS clean room: many wafer runs for process step and process module development, improvement and fine tuning, as well as in-line characterization. We succeeded developing a complete working manufacturing process flow suitable for the MEMS design discussed above. These results have been applied to the manufacturing of actively addressed MMA chips. First wafer lots of these active MMAs have been finished.

The third topic, discussed in Chapter 4, is the packaging of these actively addressed MMAs. Packaging of such a chip is quite challenging, as it has to fulfil high standards regarding very high bandwidth signal quality, protection of the sensitive MEMS mirrors while allowing optical access to them, proper cooling of the backplane while keeping a good mirror area planarity, and more. We succeeded in developing a packaging concept and process flow meeting all these requirements.

The fourth topic, discussed in Chapter 5, is the characterization of various MMA chips. Due to some delays in the previous steps, the active MMA chips could not be operated as designed, yet. Instead, a passive addressing method has been set up that allows deflecting all the pixels with a common DC voltage applied to the stator. This at least allowed verifying the functionality of the MEMS as manufactured on CMOS backplane. We found that in good chips almost all pixels can be deflected properly and precisely. Chapter 5 also includes measurement results of other specified parameters such as local and global flatness, pixel tilt, and the like.

Even more information and details on our results can be found in the papers that we've written and presented during the project. References to these are listed at the end of this report.

In summary, the work reported here has been very successful, overcoming serious manufacturing and external issues, and has produced the first MMA chips that are working well. This proves the actuator concept and feasibility of such a high-resolution phase-modulating SLM. The achieved performance parameters are a very good starting point for fine-tuning the design and manufacturing process to develop a very high-quality commercial product.

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Chapter 1 Introduction

The demand for 3D displays for virtual, augmented and mixed reality is increasing rapidly. While there are a number of such displays already available, there is still a need for improvement of the image quality. Regular and extended use of 3D displays demands a natural visual experience with all natural depth cues, without limitations in depth perception, and especially without physiological side effects for the user like eye fatigue, depth misjudgement, motion sickness and accommodation-vergence conflict, which are known from alternative and intermediate technologies such as stereoscopic displays. The best possible solution is the full reconstruction of a natural light field by real holography for perfectly realistic images. The term 'holography' unfortunately is widely used for all kinds of displays where the screen is not obviously visible, often even for 2D imaging. In this report, we use this term in its original sense only for a display that realistically reconstructs the field of light in three dimensions just as if it came from a real object. A display, as opposed to a still image, moreover allows updating the image fast enough to show moving scenes.

The key component of such a real holographic 3D display is a spatial light modulator (SLM). For holography, the best choice is a modulator allowing a multi-level precise phase control of the incoming coherent light, see Figure 1. The huge amount of information in a hologram requires as many millions of individually addressable pixels as possible. To keep the effort at all manageable, only a small 'viewing window' for the user's eyes is provided with image content. Even then, the SLM will have quite challenging specifications.

Unfortunately, none of the currently available kinds of SLMs can meet this challenge fully. Within this project REALHOLO we are therefore developing a novel kind of MEMS (micro electro mechanical system) SLM optimized for computer generated holography (CGH) applications.

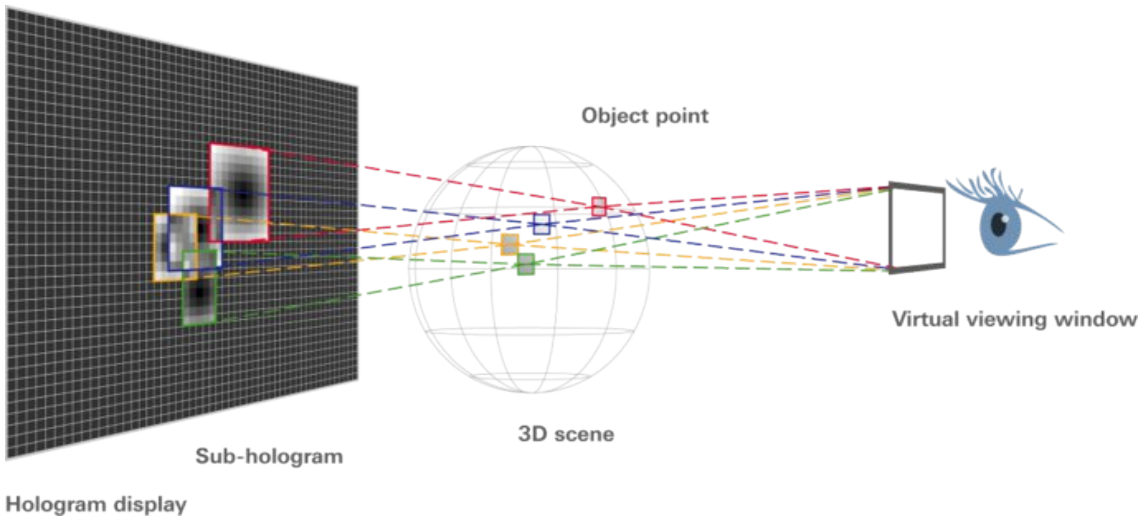


Figure 1: A piston micro mirror array can modulate coherent light to produce fully realistic 3D images correctly located in the real world

As a first application, REALHOLO is aiming for a medical holographic 3D display, see Figure 2. For a good quality holographic image, the project partners anticipate that the SLM needs to fulfil the specifications in Table 1.

Figure 2: A holographic system for medical applications to display fully realistic 3D images

Parameter	Value
pixel count	4000 x 2048
pixel size	4µm x 6µm
frame rate	> 1kHz
vertical deflection range	0 … 350nm
deflection precision	8 bit
mirror tilt	< 0.1°
pixel addressing voltage	0 … 3.3V
power dissipation	< 4W

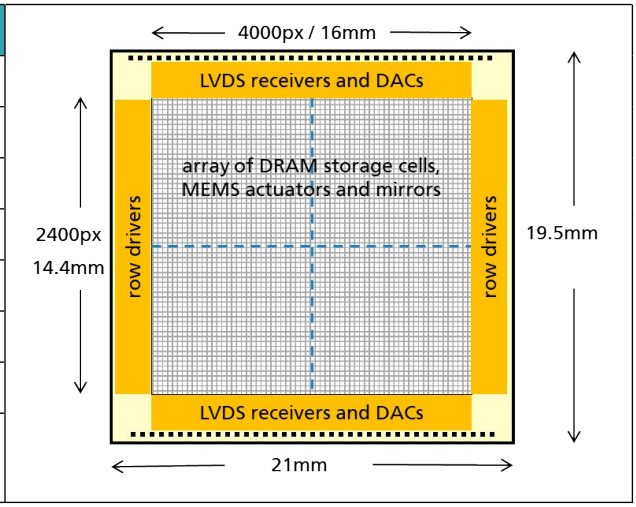


Table 1: Key SLM specifications and chip floorplan

From a MEMS point of view, we would like to have an even higher addressing voltage to get more actuator force. However, to be able to deflect all the pixels individually they need to be integrated on top of a mixed signal CMOS driving circuit (a so-called backplane) with the same pitch. Each micro mirror pixel requires its own DRAM-like cell to store its individual analogue addressing voltage. We didn't find a commercial CMOS process allowing to fit transistors for higher voltages into the space

available. At the same time, higher voltages would also increase the power dissipation, which is already challenging to comply with the limit at this voltage level considering the high data bandwidth.

The phase modulation of coherent light could in principle be achieved by existing SLMs based on LCoS (liquid crystal on silicon) technology. Compared to these, micro mirror arrays (MMAs) can have many advantages for real holography: the phase across a pixel is more uniform, there may be much less cross talk between neighbour pixels, they can be switched much faster, and they are independent from polarization. Well-known MMAs are offered by Texas Instruments as Digital Light Processing technology (DLP). These, however, have been optimized for 2D-image projection and are not well suited for holography: the pixels deflect in tilt mode instead of the piston mode preferred in holography and there are only two possible addressing states for each pixel instead of the many required here. The existing piston-mode MMAs have quite large pixels and therefore small diffraction angles and too few pixels for good quality holography.

REALHOLO is a project to develop an advanced display system for real holographic 3D mixed reality (MR) applications, structured illumination, and other, related applications. The core component of such systems is a micro-mirror-based piston-type spatial light modulator (SLM) with challenging specifications, which has not been available before this project. REALHOLO is developing this new type of SLM based on micro-mirror-array (MMA) technology in its Work Package 3.

Chapter 2 MEMS Actuator Concept

The commonly used actuation method for phase modulating micro mirrors is often using an electrostatic parallel-plate actuator. This approach is not suitable for this application. A stroke of about 350nm would need a vertical gap of around 1.8µm to reliably avoid the electrostatic pull-in phenomena. This, however, would result in only a very small force with the available voltage budget, which then would lead to a very fragile hinge design. The non-linearity of the response curve means that at large deflections the voltage has to be extremely precise for a required precision of the actuator position. Figure 3 does give an example with a bias voltage of 3.3V.

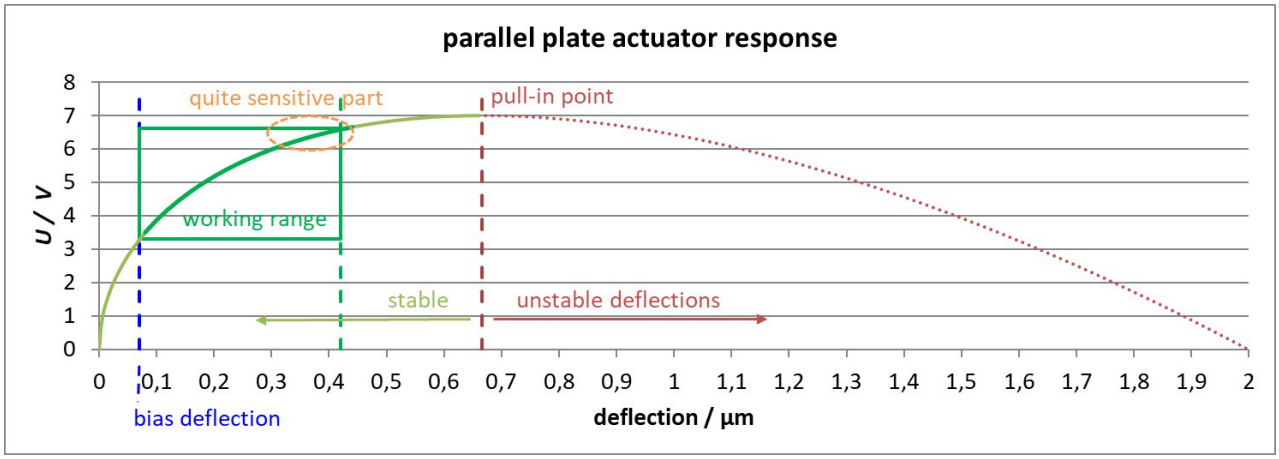


Figure 3: response curve of a parallel plate actuator with the planned parameters, including a bias voltage of 3.3V

Furthermore, the crosstalk between neighboring pixels would be quite large, depending on the deflection position of the two pixels, since the gap between the top and bottom electrode is almost 50% of the pixel width. In the worst case it could be above 10%, which would make the required deflection precision of 8bit completely out of reach.

Due to those negative points we optimized a comb drive type actuator, see Figure 4 and [15], which is a rather new concept for closely packed micro mirror arrays. For a comb-drive actuation there is no electro-static pull-in in the stroke direction since the force in the deflection direction does have a maximum and is then reduced again when getting closer to having the yoke in plane with the stator electrode. Therefore, the electrodes can be much closer together and the obtainable forces are about a factor of 10 larger compared to the parallel plate type.

The concepts in the figure still have some issues: even a small overlay mismatch between yoke and stator plate would result in a tilting motion of the mirror. Also, the electric field might induce charging of the oxide layer underneath the stator electrode, which then will influence the deflection curve and reduce the precision.

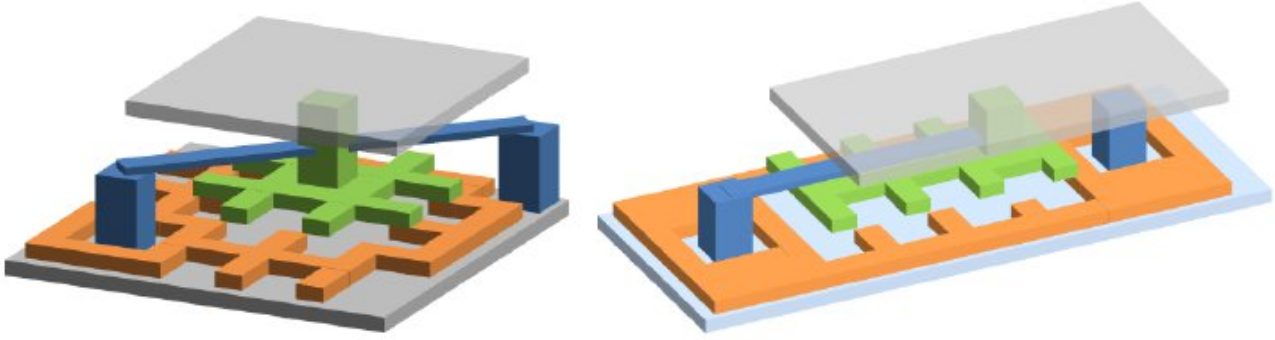


Figure 4: Sketches of some of the first concepts of comb-drive devised in this project

To improve on those issues, we came up with the comb drive actuator and design shown in Figure 5. The deflection of the mirror is now guided by two hinges in different MEMS layer that act as a parallelogram guide for the mirror, see Figure 5 and [16]. Therefore, the tilt from possible overlay mismatches will be rather small.

The CMOS addressing circuitry will be connected to the lower half of the actuator. It consists of a base plate (cyan in the figure), lower hinge (dark blue), and yoke (green). Those elements are all carrying the address voltage supplied by the CMOS so there is no electric field in between them and there is also no oxide present and therefore no charges induced.

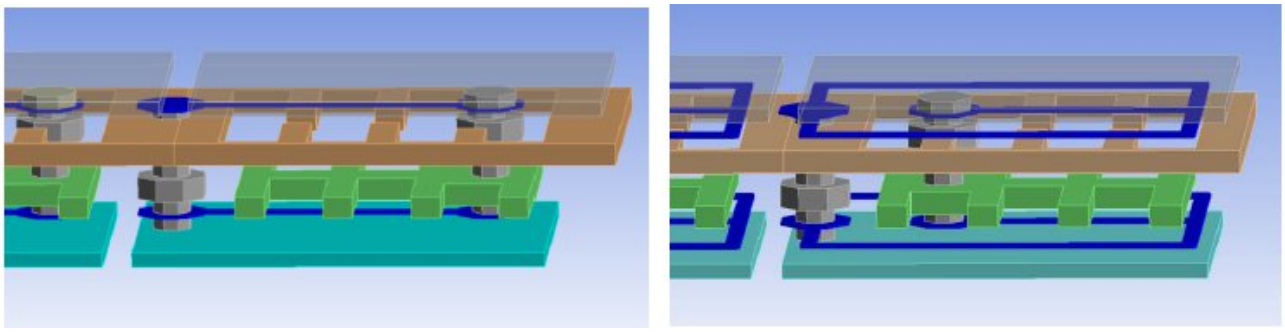


Figure 5: Improved comb drive design with a straight hinge (left) or a Q-type hinge (right)

The dual hinges stabilize the mirror during actuation quite well, and also against stress gradients in the hinges themselves. We did a comparison simulation between a single hinge and the double hinges under different stress situations, shown in Figure 6

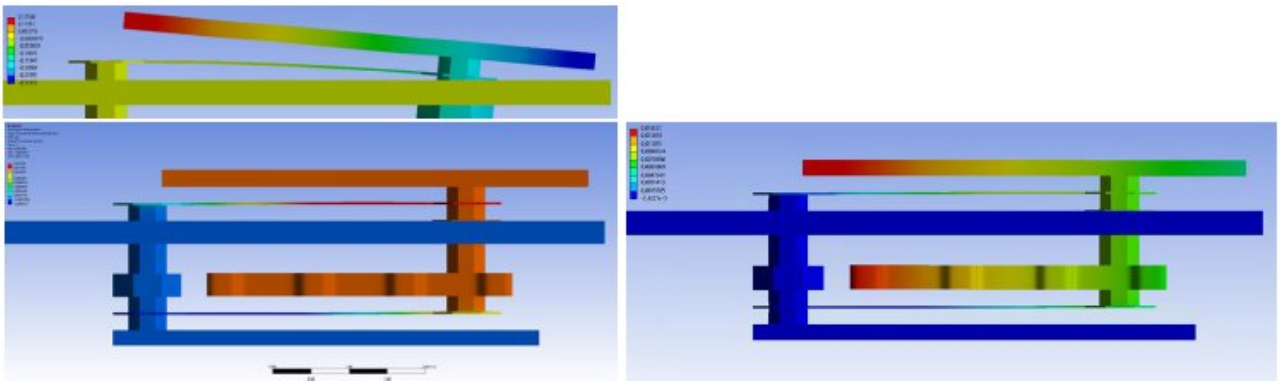


Figure 6: Comparison of tilt for a single hinge with an example stress gradient of 100MPa (top picture, tilt: 4.8°) to a double hinge design where both hinges have the same stress gradient (lower left picture, tilt:0.0°) and a double hinge design with a 100MPa stress mismatch in the two hinges (lower right picture, tilt:0.6°)

The spring stiffness of those hinges scales roughly with thickness cubed. So, the version with dual hinges still allows about 79% of its original thickness.

Calculating the response curve of the actuator is not straight-forward. Both the electrostatic force F_{el} between the stator and the yoke parts and the mechanical force F_{mec} of the spring together define this. However, it takes a high effort to assess these from different physical domains within the same finite element method (FEM) simulation run. Therefore, simulations were performed for these two forces independently and we get the response curves later from the force equilibrium.

The electrostatic force F_{el} in the actuator is simulated in a surrounding air box whose dimension is equal to the pixel size. This box has mirror boundary conditions, so the effect of the neighboring pixel geometry is implicitly considered here for the same addressing state (for cross-talk simulations see below). The simulations are all performed for a specific potential difference U_{ref} between the yoke and the stator for a number of yoke positions. The resulting curve can then be scaled to any other addressing voltage as the electrostatic force is proportional to the voltage squared for a given geometry.

The mechanical force F_{mec} is found from static structural simulations by applying various loads to the FEM model. We find a very good linearity for the full range of design parameters and deflections, meaning that we operate within Hook's law. Therefore, the stiffness can be calculated as a spring constant.

Figure 7 shows an example of F_{el} curves for different potential difference at various yoke positions, as well as an example straight line for F_{mec}. Each point where the F_{mec} line intersects a F_{el} curve represents the force equilibrium for the respective voltage and position. The actuator response curve is generated from these intersection points of the two force curves.

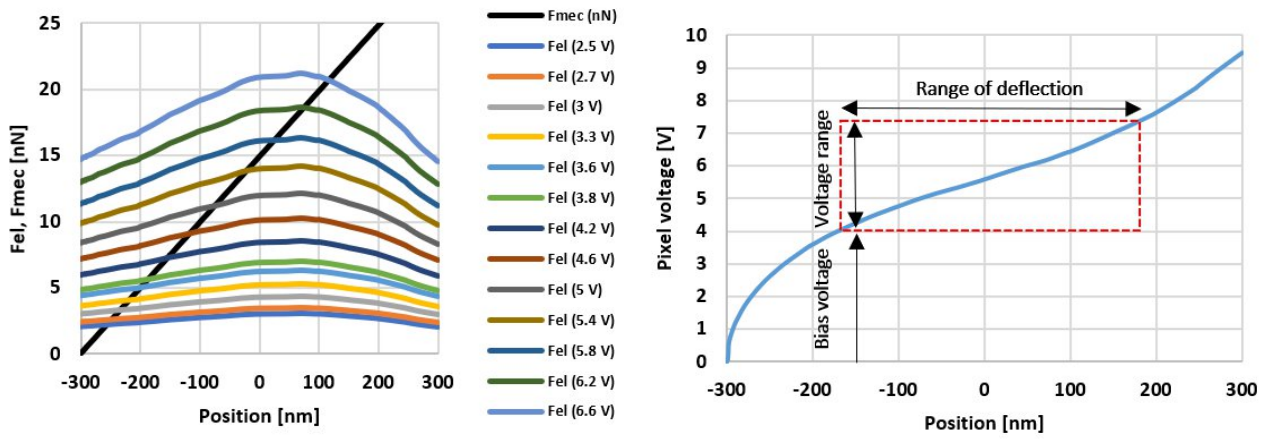


Figure 7: left: simulated data for F_{el} and an example F_{mec} and right: calculated response curve (voltage vs position) using the force equilibrium points with 'box of operation'

As a zero point for the position axis we chose the situation where the upper face of the yoke and the lower face of the stator lie in the same plane. In this example geometry the stator and the yoke have a thickness of 300 nm each and thus are fully overlapped at position 300 nm. One would expect the electrostatic force to be zero at this position due to symmetry, but obviously the asymmetric surrounding of the combs – the base plate below at yoke potential and the mirror above at stator potential – still has a very strong impact so that the simulated Fel is reaching zero only at a much larger deflection.

The red box in Figure 7 indicates an operating region of 350 nm. The lower edge of the box is given by the bias voltage that is common for all pixels of a device and constant in time. The height of the box represents the required operating voltage range which is individual for each pixel. This operating voltage range is limited by the voltage that the backplane CMOS circuitry can provide (3.3V). Note the small deviation of the response curve from being linear within the box of operation. This ensures a good precision of the actuator positions at all addressing voltages for our comb drive actuator.

Due to the large open space between the stator and the base plate we also investigated a possible electrostatic crosstalk between neighbouring pixels. To do this the geometric structures were enclosed in a prismatic simulation volume, and two pixels were placed next to each other sharing the long edge (see Figure 8). To evaluate the crosstalk, the electrostatic force was evaluated at one pixel (the sensing pixel) and the position and voltage of the other pixel (the probe pixel) was set to either top or bottom position. At the top position the voltage at the yoke and base plate is 6.6V, whereas at the bottom position the voltage there is 3.3V. The sensing pixel was kept in the top position with 6.6V applied to its yoke and base plate.

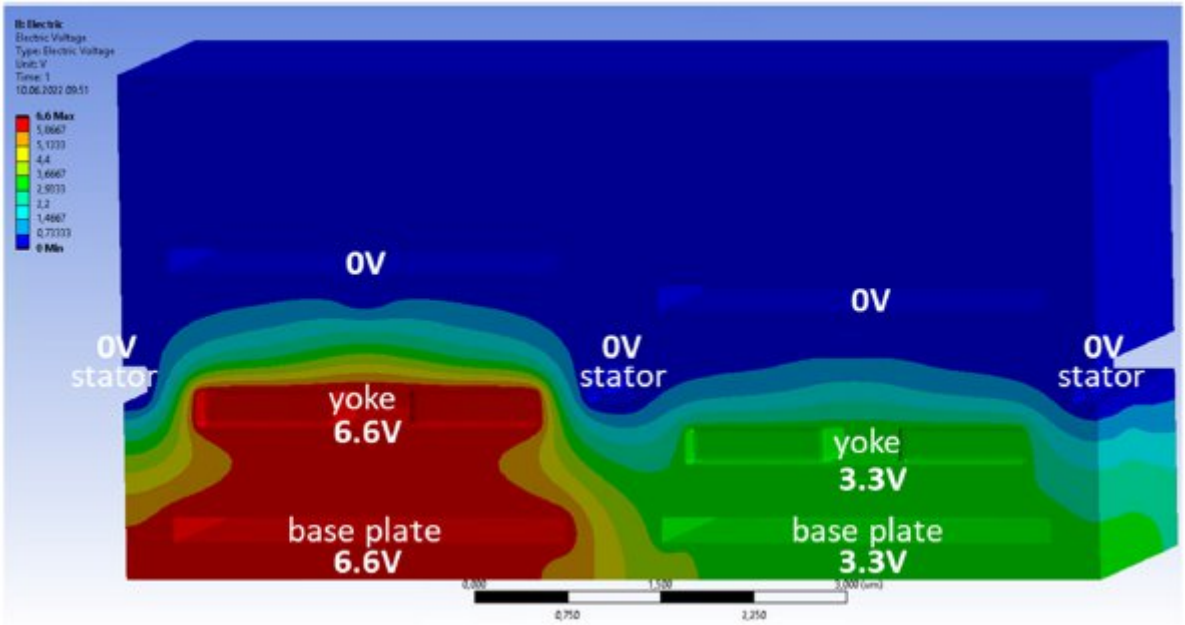


Figure 8: Cross-section through the simulation volume for the crosstalk simulations. Shown are the voltages throughout the air space. The labelled voltages are the ones that are applied to those structural surfaces

The original design had a crosstalk of about 0.65%. This means the force amplitude at the sensing pixel did vary by this percentage depending on the deflection state of the neighbouring pixel. This does not sound much, but the other neighbour pixel would have the same influence while the specified deflection accuracy needs a crosstalk variation of much less than 0.4%. To achieve this we investigated different geometric variants: shorter comb fingers, reducing the width of the base plate, extending the edge of the base plate upwards, extending the main stator axis downwards, adding a shielding ring in the same layer as the yoke. For a detailed analysis of the different variants please see [8].

Those changes did all bring gradual improvements to the crosstalk. The final variant with the shield ring was then also the best and the crosstalk simulation there did show a force difference of close to 0.0%. Figure 9 shows a design with this shield ring. It is made in the yoke layer and doesn't require any extra fabrication steps.

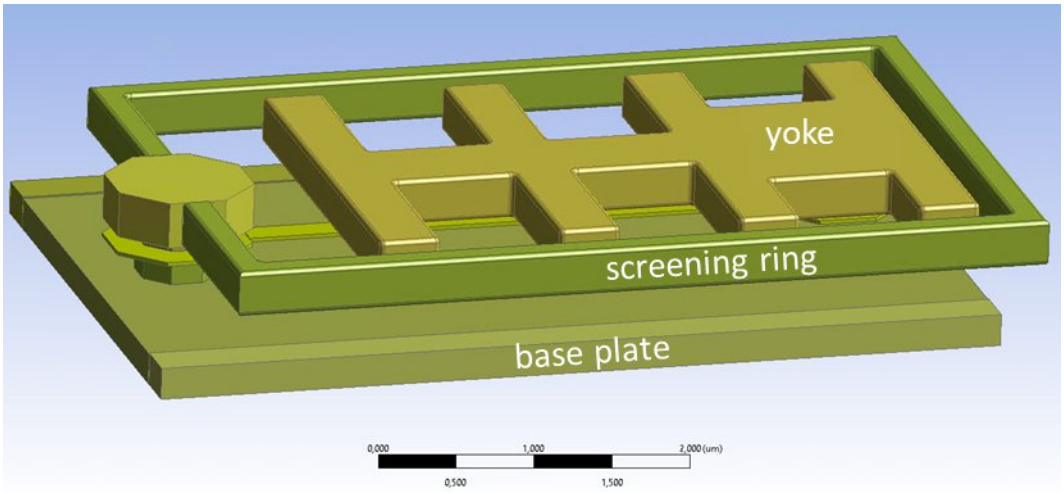


Figure 9: Placement of screening ring within the same layer as the yoke. Shown are only the layers up to the yoke layer

In Figure 10 a cross-sectional view shows the voltage distribution within the pixels. The high voltage of the left pixel is nicely confined within its own volume space. For further details please see [8].

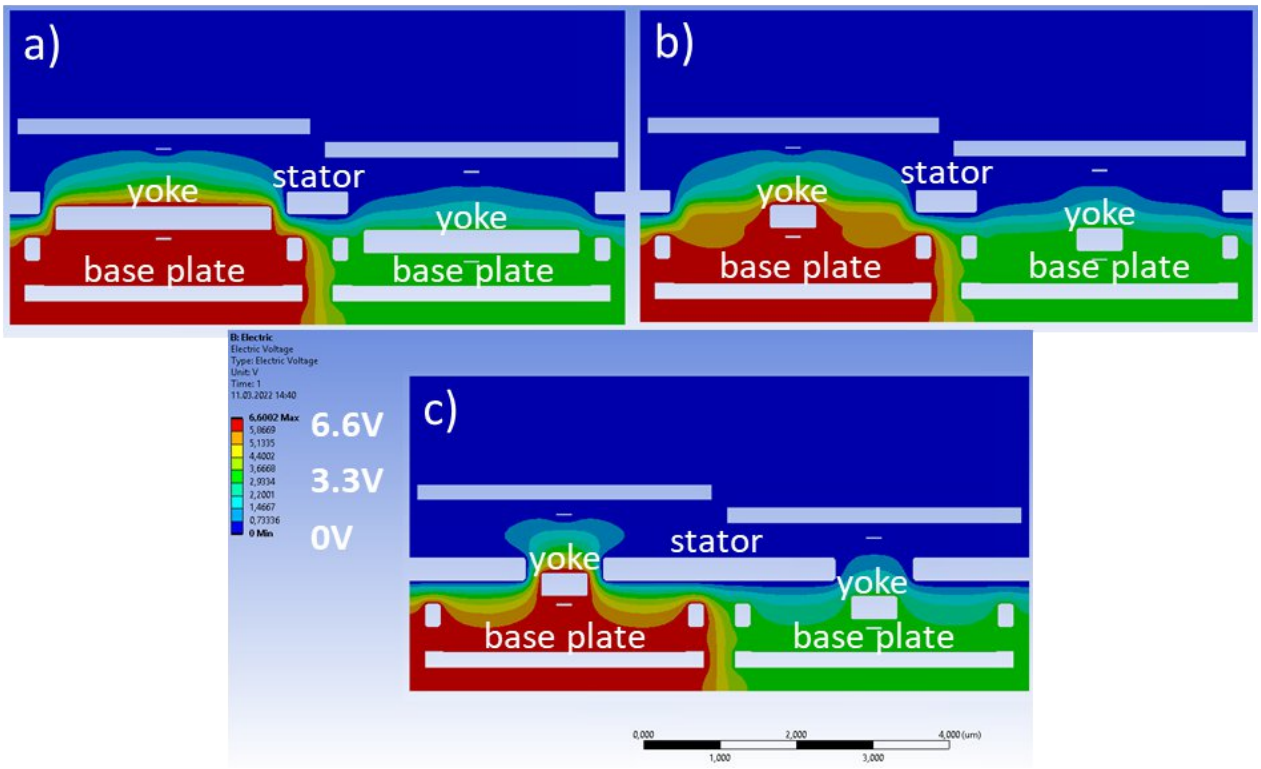


Figure 10: Cross-sectional voltage distribution of the geometry with screening ring at three different lateral positions. A) cross section through a yoke finger, b) cross-section through the lateral gap between yoke and stator finger, and c) cross-section through a stator finger

As a final design variation step we also investigated whether the DUV lithography tool newly available at that time would allow for a better design. During this work a new 5 finger design was established (see Figure 11 and [7]). The additional finger on the yoke structure did result in a larger force available which allows for hinges with a larger spring stiffness. This larger stiffness can be used to increase the hinge thickness and increase overall stability.

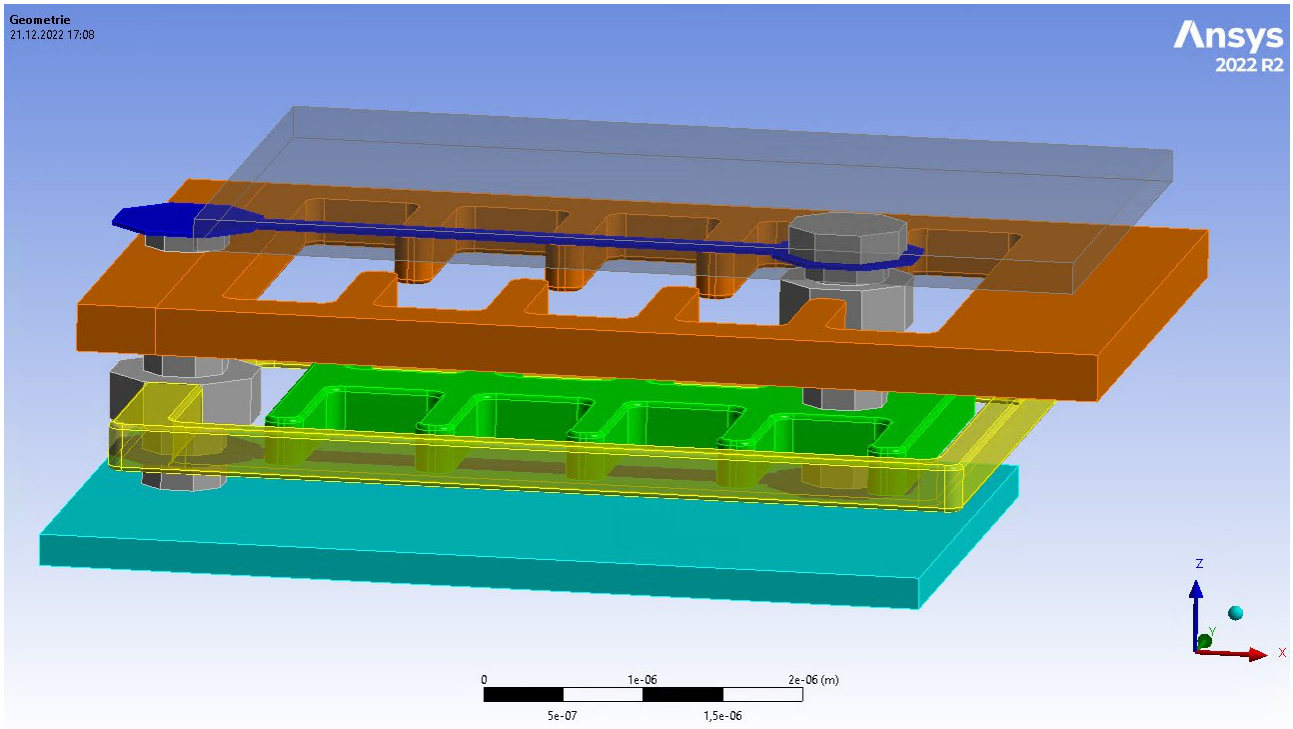


Figure 11: Final design with 5 fingers on each side of the yoke

Chapter 3 MEMS Manufacturing

3.1 Process flow

The MEMS actuator and mirror are manufactured on a wafer after the addressing circuitry has been made by a regular CMOS foundry (X-FAB) as partner of the REALHOLO project. This is done layer-by layer in a clean room of Fraunhofer IPMS with processes similar to standard CMOS fabrication. In general, structural and sacrificial layers are deposited and patterned alternatingly and the sacrificial layers are planarized by CMP to get precise results. In a final step, the sacrificial layers are removed leaving the designed actuator structure free to move according to the electrostatic addressing.

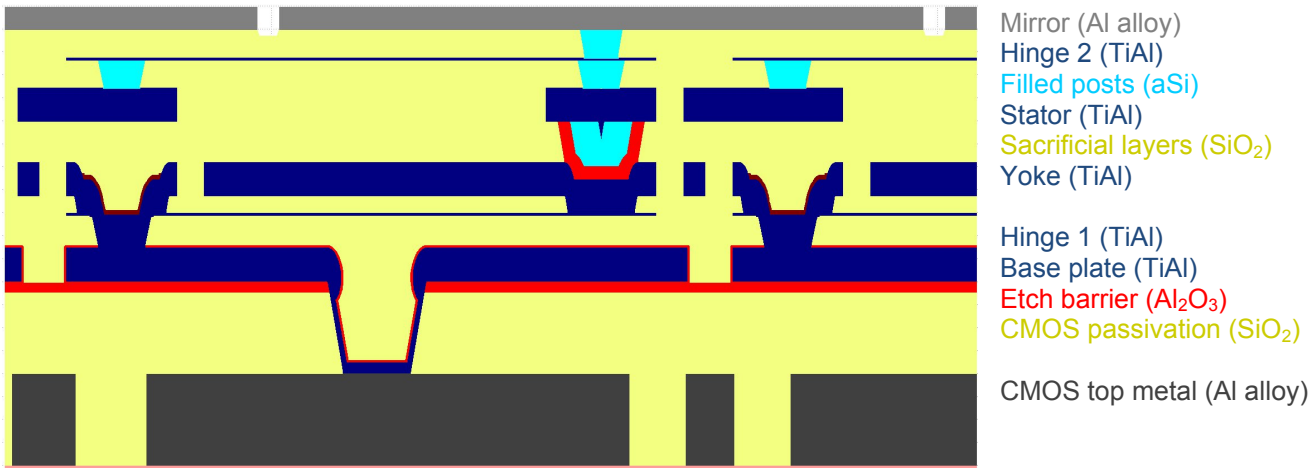


Figure 12: schematic cross-section of the MEMS-part.

3.2 Wafer processing

The wafer processing had several challenges in the different parts of the actuator, most of them related to extreme requirements on uniformity of CD, overlay and thickness. While the last one was an optimization of deposition processes mainly, the two other ones are mainly lithography related. Here at the beginning of the project Fraunhofer IPMS could only rely on i-line lithography, with typical technical limits. Just later DUV-lithography became available in the Fraunhofer IPMS clean room, offering much better possibilities, allowing shrinking of feature sizes, but also came with a lot of challenges, since it was a totally new technology Fraunhofer IPMS had no experience with. In the following section process development and measured of several parts of the actuator are discussed.

3.2.1 Springs

3.2.1.1 Deposition

The first part to discuss are the springs. Even more so than the CD-uniformity of the spring width, the thickness of the spring is crucial for its stiffness and response to applied voltage. Simulations showed, that the 32nm total thickness, consisting of 28nm TiAl and 2nm Al_2O_3 underneath and above for passivation, should be a suitable value for the final AHS design. Even with some margin in the case of variations of the CD values mentioned in the previous section, the full stroke for red light is reachable within in the CMOS parameters. A slightly better linearity might be achieved by thicker springs, at the cost of possible stroke limitations.

It was decided to split wafer lots, AHS#1a using a total thickness of 32nm and 36nm, respectively. The later lots where split 32nm/34nm. Depending on the conditions of the sputter target, the deposition rate changes and must be adapted for each lot. The long-term monitoring of for sputtering

of such ultra-thin layers is still work in progress and it is still a big challenge to exactly hit the target value and achieve best uniformity. As shown in Figure 13, for AHS#1a the prediction of the sputter process worked well, getting 32.2nm and 36.7nm average thickness. For the next lots the deposition rates where overestimated, resulting in lower than aimed thickness. Just for AHS#3b, we could return to a good prediction and hit the target values with 32.0 and 34.1nm quite well.

Looking on the uniformity of the spring thickness, usually values close to or even lower than 1.0nm range can be achieved over a full wafer. Usually, the lower thickness values are close to the wafer center with a small shift in south-east direction. This is due to the specific characteristics of the sputter chamber. The best uniformity per chip is then also achieved for the chip in this region with a total variation of <0.1nm. The highest thicknesses occur around a 60mm radius range, with chips in this region still showing acceptable thickness variations of <0.2nm. Chips between the center and half-radius can show increased thickness variation up to 0.4nm. Towards the wafer edge, the thickness decreases again. The distribution can be changed, for a better levelling between center and half-radius at the cost of worse chips at the outer wafer region. Thus, setting the best parameters every time is a challenging trade-off between best thickness conformity, uniformity and yield per wafer.

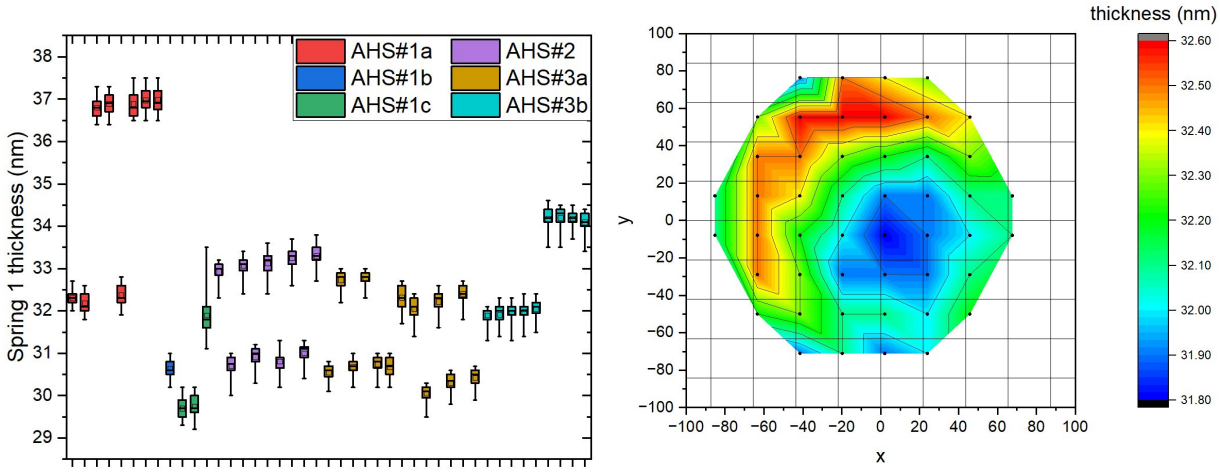


Figure 13: Optical measurement of spring 1 thickness. Left: Box plot per wafer for all lots. Right: Typical thickness distribution on the wafer.

Another issue occurred in early lots was an effect of buckling of the springs after release. In early trials it was found, that pure TiAl is very sensitive to oxidation at subsequent CVD processes but also HF vapor of CF4/O2-plasma used for the release. Such oxidation causes heavy stress and stress gradients in the spring since even a 5nm oxidation layer is a crucial part of the total thickness. Replacing 2nm of TiAl top/down of the spring by Al2O3 improved the situation, however thereafter even in the later PHS/AHS lots there were small steps of development trying to replace PVD-Al2O3 partly by ALD-Al2O3 and increase the thickness of the passivation layer in sub-nanometer steps to get optimal passivation without exceeding the limits of spring stiffness. Together with the changes in sacrificial layer thicknesses (described in 3.2.4.1) a significant reduction of buckling induced sticking pixels could be achieved, leading to a stable yield of >90% of movable pixels in the last PHS lots #4 and #5 as well as the very first AHS lot. However, due to delays in characterization a final configuration of TiAl and passivation layers is still a matter of fine-tuning.

3.2.1.2 Lithography and patterning

At the beginning of the project, we relied fully on i-line lithography. The testing vehicle HTC used 400nm wide springs in 3 different configurations (straight, Q-springs, C-springs). Later, on PHS we could reduce the width to 200/300nm at PHS and used a final CD of 240nm for AHS. The possibility of DUV-lithography helped a lot, since pattern fidelity was greatly improved. In Figure 14 the difference of a Q-spring from a HTC patterned by i-line can be compared to a Q-spring from PHS patterned by DUV.

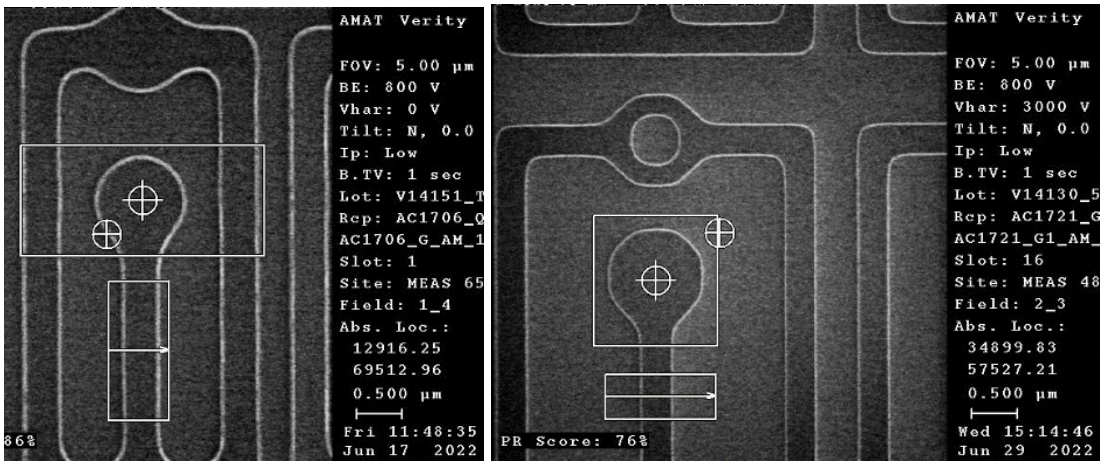


Figure 14: Left: SEM-image of a patterned 400nm Q-spring from the HTC design patterned by i-Line lithography. Right: SEM-image of a patterned 300nm Q-spring from the PHS design patterned by DUV-lithography.

Besides pattern fidelity the imaging performance of the MMA device also depends on the CD-uniformity of the springs. Here intensive development for finding the optimal parameter set of resist thickness and exposure parameters was done like for no other layer. As outcome we could reach a stable process keeping the CD close to the design value of 240nm as well as reach a CD-uniformity (3 sigma) of ~4% per chip for all AHS lots, as shown in Figure 15. This should result in a very uniform actuator response over the full MMA.

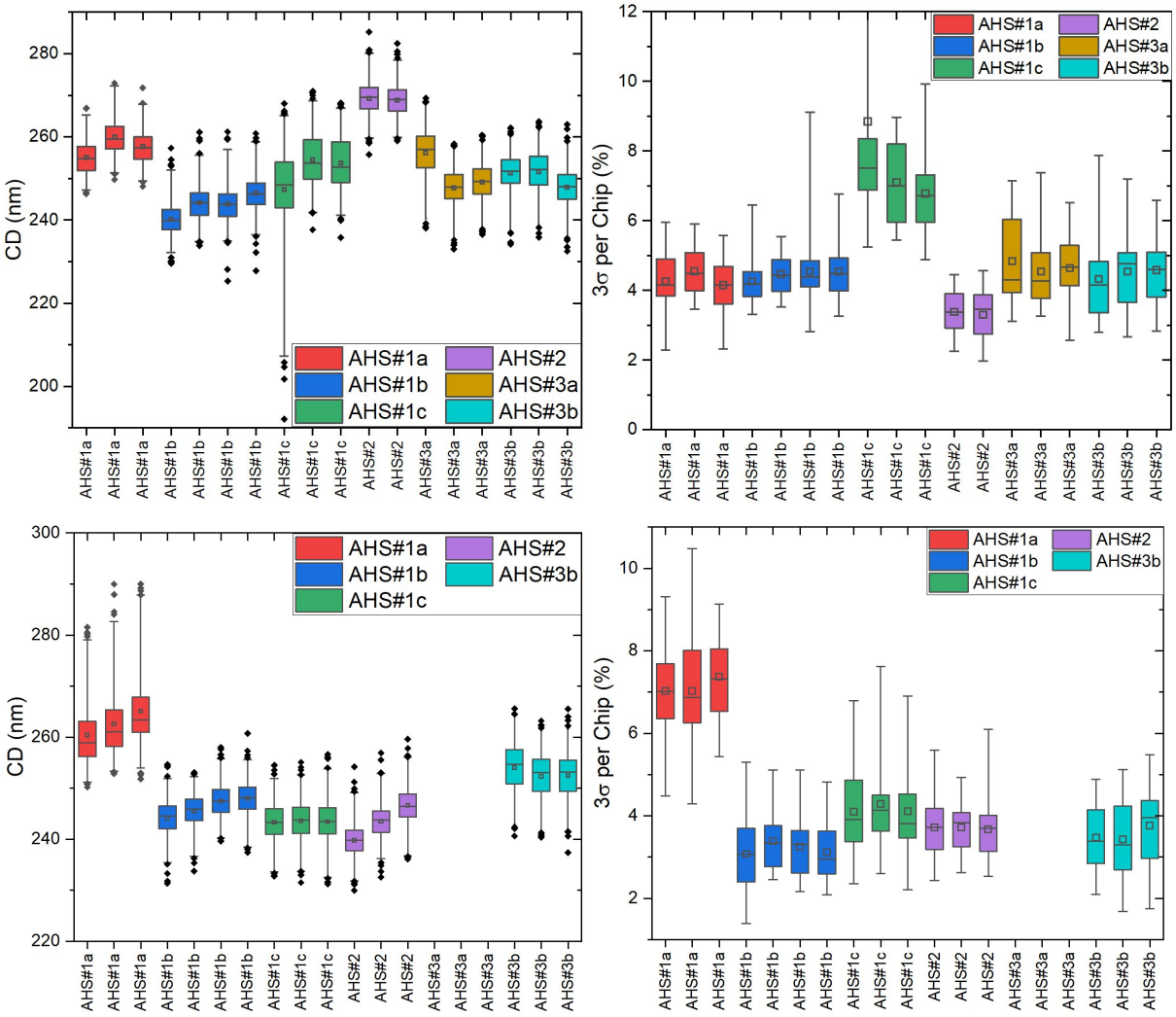


Figure 15: CD per wafer (left) and CD-uniformity per chip (right) of spring1 (top) and spring2 (bottom).

3.2.2 Yoke/Stator

3.2.2.1 Patterning

Similar to the springs, we started with an i-line only design on HTC with fingers of 400nm width. Later with availability of DUV-lithography we reduced the finger width and increased the number of fingers, resulting in a higher electric force. For the yoke and the stator, we have two different basic configurations, with 4 fingers or 5 fingers, respectively. Each of these has two variants, one with extra narrow fingers and thus larger horizontal gap between the stator and yoke and one with slightly smaller gap and wider fingers. The different designs and configurations are shown in Figure 16 (4-finger) and Figure 17 (5-finger). The 4-finger design is more conservative, with a finger with of 400nm and 360nm. For this the exposure and patterning is less challenging, but of course we gain the better overlay performance of the DUV-scanner compared to former i-Line-stepper. The 5-finger design reduces finger width to 280nm and 240nm, making patterning more challenging with respect to CD-uniformity and corner-rounding. Furthermore, it incorporates the seal-ring with only 200nm CD and small distance to the fingers. These make the process development much more complex than for the 4-finger design. On the final AHS only the 5-finger design was applied.

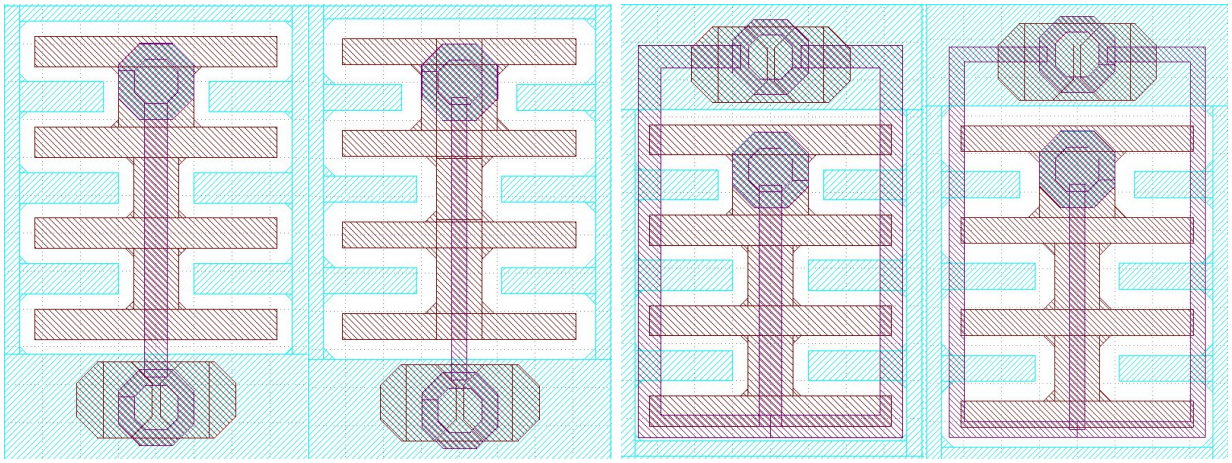


Figure 16: Layout for the 4-Finger design with spring (purple), yoke (red) and stator (turquoise). From left to right: 300nm straight spring, 200nm straight spring, 300nm Q-spring and 200nm Q-spring.

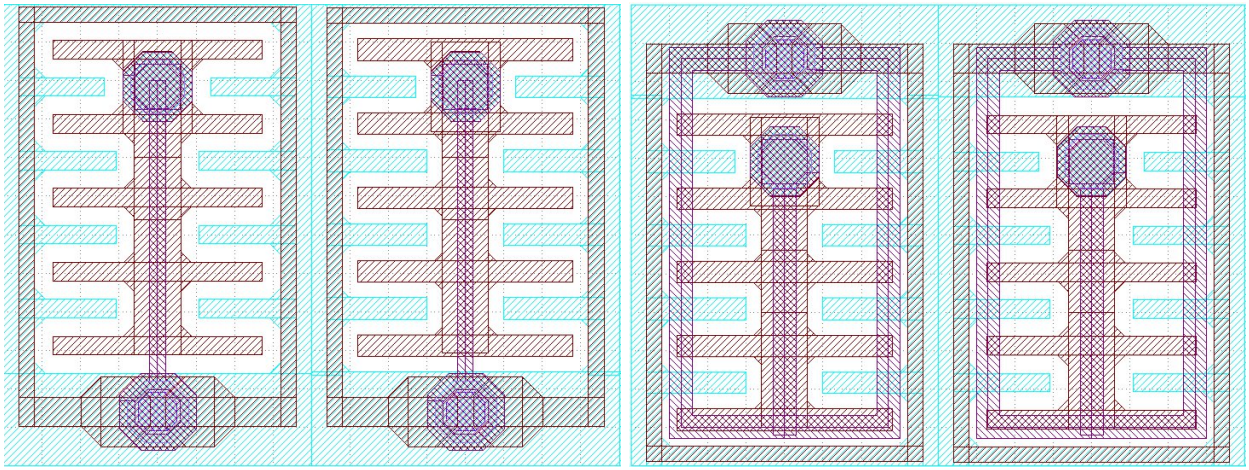


Figure 17: Layout for the 5-Finger design with shield ring (brown). From left to right: straight spring with 240nm gap, straight spring with 200nm gap, Q-spring with 200nm gap, and Q-spring with 240nm gap.

Regarding etching, we observed that the metal-RIE process already used with i-Line performed very well even with the new DUV-BARC/resist combination. For both yoke as well as stator we got very steep sidewalls, low overetch and no additional loss in corner-rounding compared to the resist mask

We only observed a CD-loss of 10nm compared to the resist, but this will later be compensated by a smaller dose during exposure. From the results of both single layers we expect very nice results for the full devices especially compared to the former i-Line processes used in the HTC preparation. With the improved overlay of the DUV-scanner, the final combination should look like the image composition shown in Figure 18, representing a good pattern fidelity of the fingers.

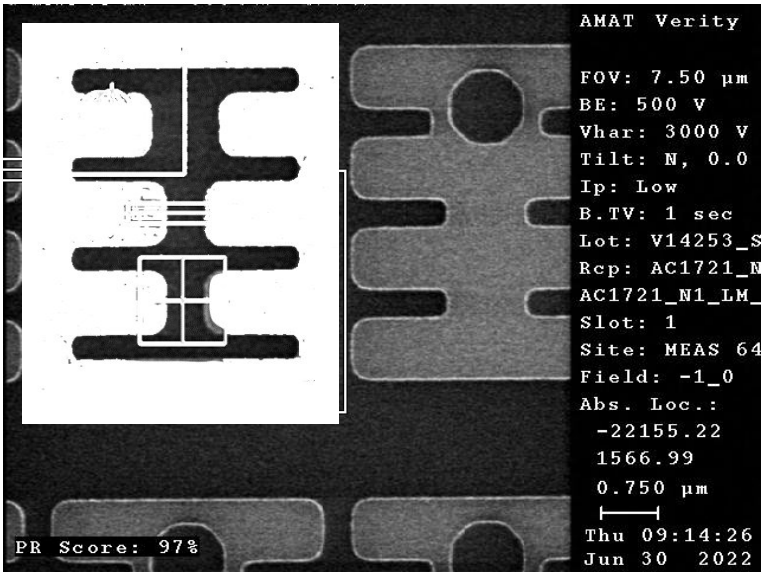


Figure 18: Overlay of SEM-images from 4-finger yoke and stator.

The development of the 5-finger design only resulted in small changes of the parameters. We could keep the same etching process but need to adapt the exposure conditions. However, on blank wafers as well as PHS lots the pattern fidelity was still good even with the shrinkage of the finger width, as shown in Figure 19. Later in AHS we suffered from problems with depth of focus due to the CMOS topology. This issue could be solved, even with some loss of good chips and additional delay in the manufacturing process. Details for this optimization are presented later in 3.2.6. This additional development on AHS is also represented in Figure 20, were the first wafer of AHS#1a and the full lot AHS#1b was used for process optimization for yoke exposure and patterning. However, for the later lot we managed to stabilize the process, keeping the CD of the fingers (as well as the x-talk ring) close to the specification, as well as obtain a CD-uniformity of <8nm per wafer.

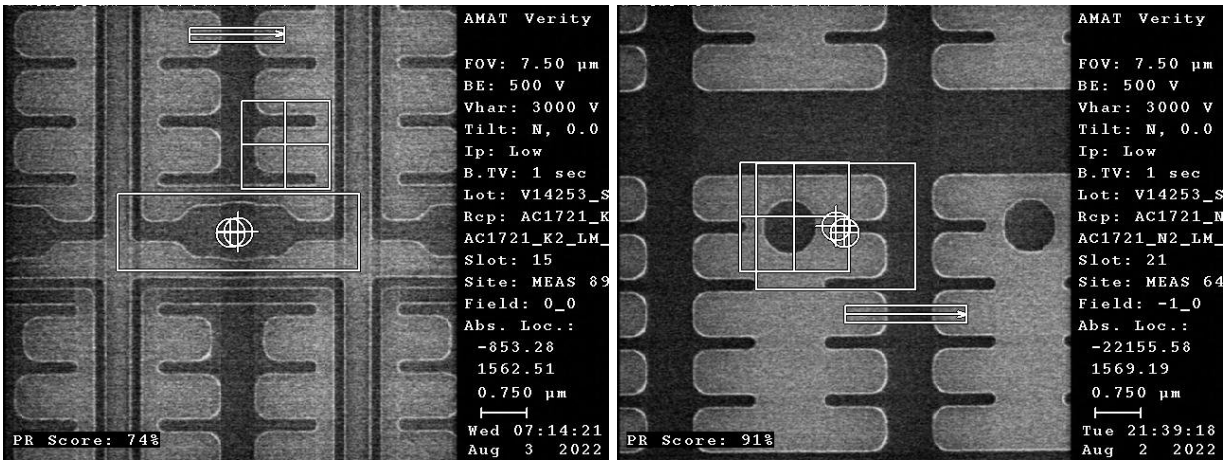


Figure 19: Focus-Exposure Matrix for the 5-finger yoke (left) and stator (right) showing resulting CD of 240nm fingers.

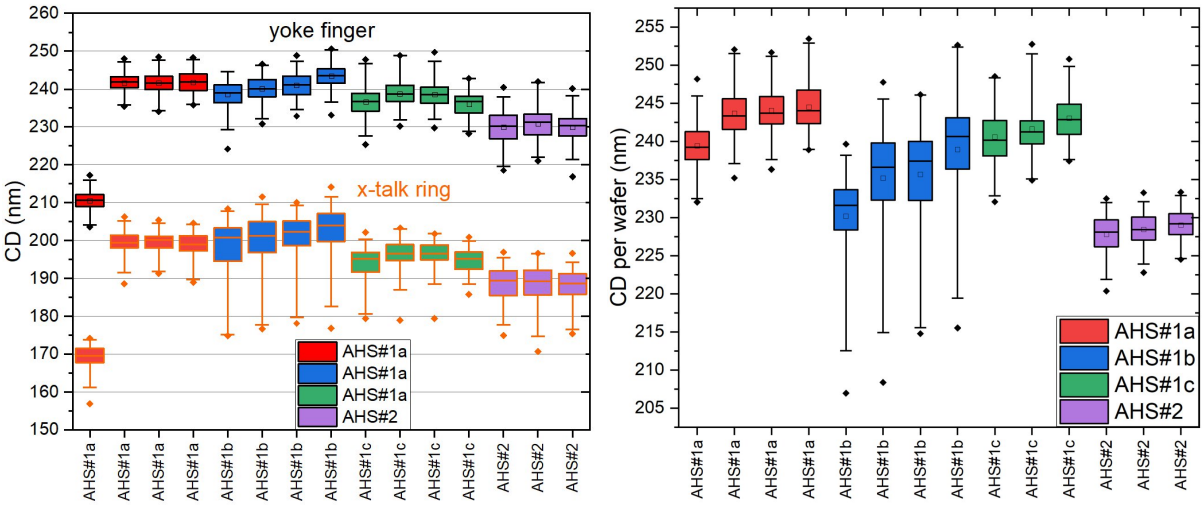


Figure 20: CD per wafer of the yoke finger width and the x-talk ring width (left) and the stator finger width (right) for all AHS lots prepared yet at the corresponding layer.

Especially in the yoke and stator layers the benefits of DUV-lithography can be seen. Beside the lower CD values and better uniformity, there was a great improvement of the overlay between both layers. This is crucial since the fingers of both parts have to move symmetrically inside each other for an optimal response curve. In Figure 21 one can see the improvement in overlay between HTC (blue part) with values no better than ±50nm, and the later PHS (purple part) starting at ±40nm and later improved to even ±15nm in resist. Due to the topography of the CMOS a certain deviation for pattern overlay in the AHS devices was unavoidable. However, as shown in Figure 22, we could keep the on-product overlay within the necessary specification of ±30nm for nearly all chips and even ±15nm was possible for a 50% share of the chips.

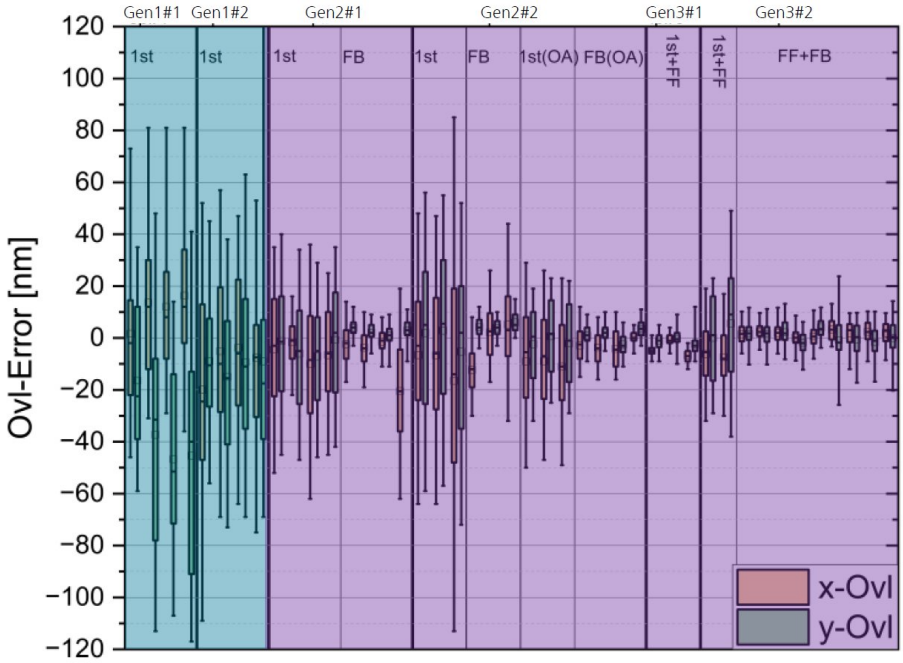


Figure 21: Overlay between yoke and stator improvement over time. Gen1 marked by blue background corresponds to HTC patterned by i-Line lithography, while Gen2 (PHS, 4-finger) and Gen3 (PHS, 5-finger) are marked by purple background for using DUV-lithography.

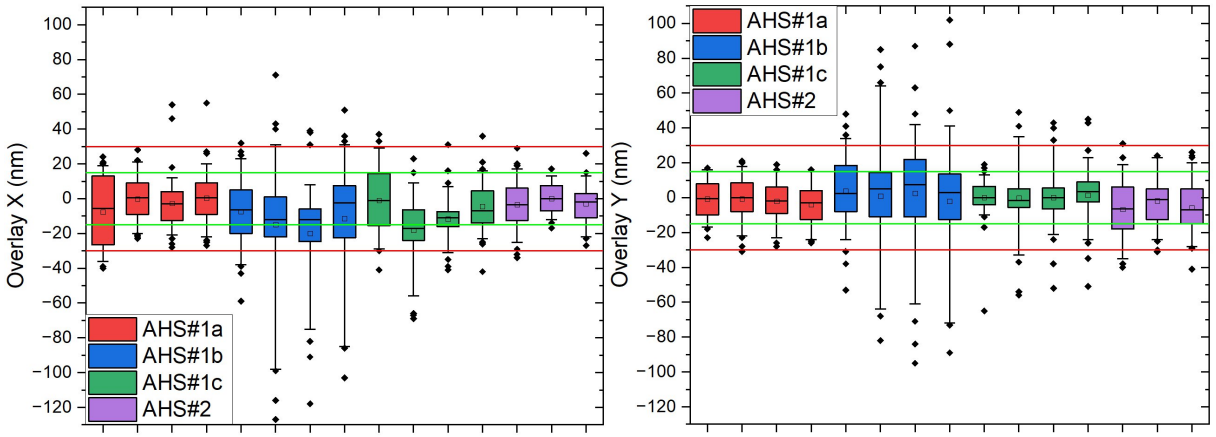


Figure 22: Overlay error between yoke and stator after patterning in X-direction (left) and Y-direction (right). The necessary specification of 30nm and the aimed specification of 15nm are indicated by horizontal lines.

3.2.2.2 Planarity

Similar to the springs, the yoke and the stator should not bend too much, to ensure a proper and uniform response curve. Unlike for the springs, the test structures on the HTC-design work well for yoke/stator due to their higher stiffness. Originally both layers were planned to consist of 300nm TiAl only. Since later we switched to a 2-step CMP process for SAC3 and SAC4, a CMP-stop layer of 40nm TiN was applied on top of the TiAl. The TiN is removed in the later course of the process and thus is not part of the final device. However, chemical reactions between TiN and TiAl or degradation of the TiAl during the TiN-removal can cause additional stress gradients in the structure. We tested both variants, 300nm TiAl only and 300nm TiAl with removed TiN. For the first case, the WLI-data are visualized in Figure 23. One can see that the paddle bend upwards by only 13nm. The bending in the case of removed TiN was 3nm downwards. Both values are very small, especially since the test structures are made softer than the final yoke/stator construction in the MMA. Therefore, and unlike for the springs we are not expecting any issues from planarity for yoke and stator.

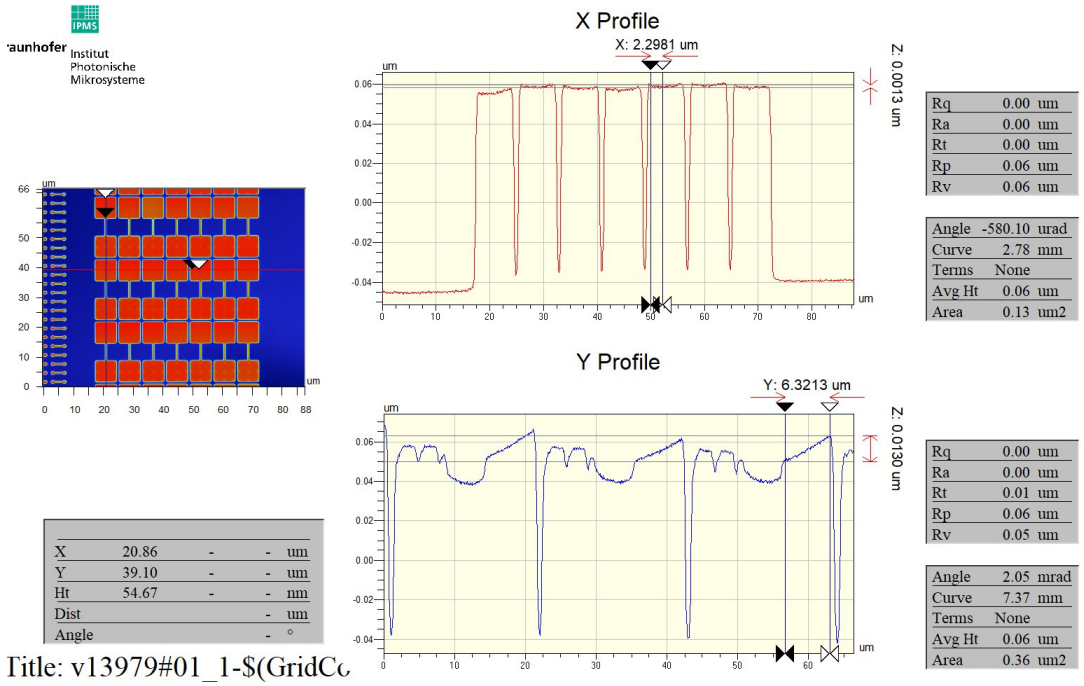


Figure 23: Visualization of WLI-data for test-structures representing the yoke/stator stack of 300nm TiAl.

3.2.3 Mirror

Next we discuss the pattering of the mirror using DUV lithography. While the former process used for HTC was an i-line process allowing a minimal width of the mirror slits of 400nm, DUV theoretically can be scaled down to 110nm. However, to improve the precision and homogeneity of the slit width, we decided to decrease the CD only to 200nm, which still is an increase of the mirror fill factor from 84% to 92%. The outcome of the new process in comparison to the i-line process is shown in Figure 24.

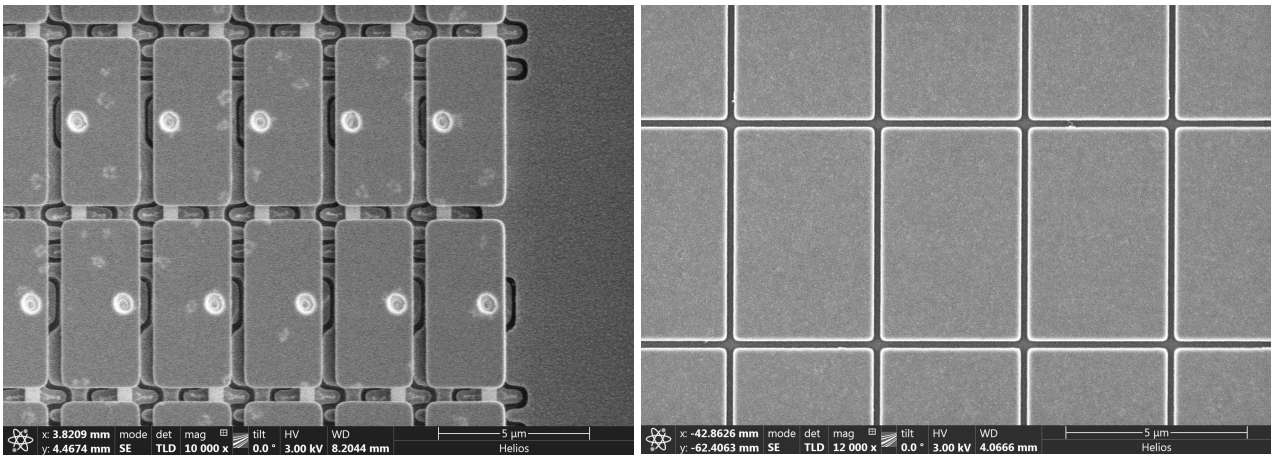


Figure 24: SEM top view comparing the 3µm x 6µm HTC-mirror patterned by i-line lithography (and with open mirror posts, left) and the 4µm x 6µm PHS-mirror patterned by DUV lithography (right).

The process itself is quire stable for a CD of 200nm with an uniformity of ±10nm obtained as presented in Figure 25. Even a further reduction of the slit width to increase fill factor in the future may be feasible.

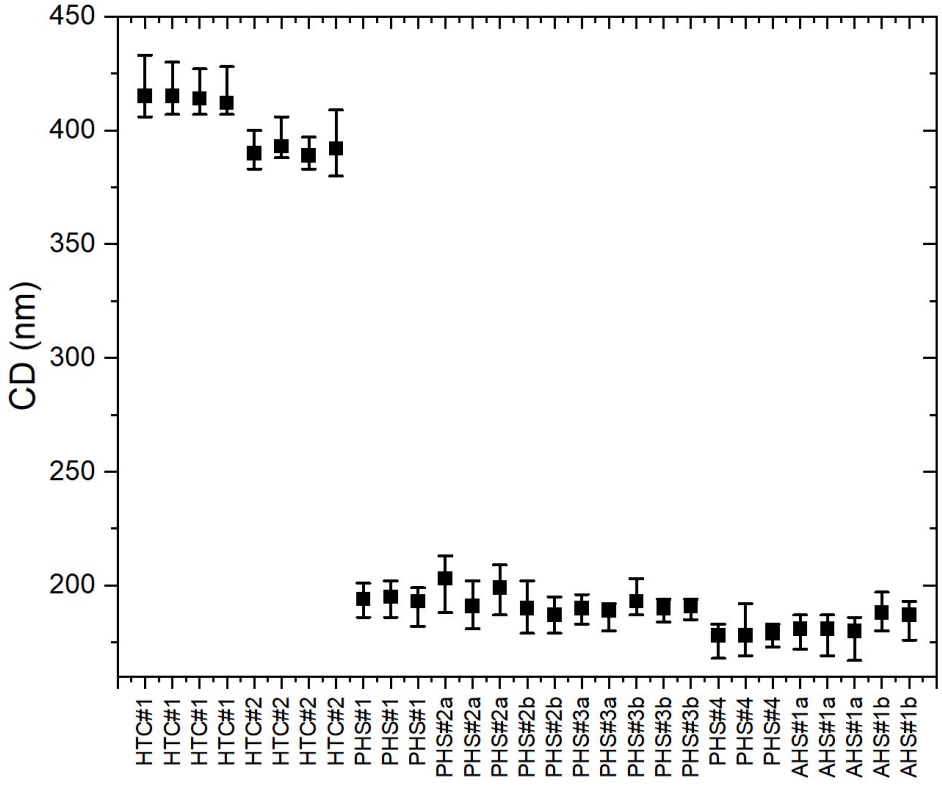


Figure 25: Measured CD for the mirror slit for all lots finishing the wafer processing yet.

3.2.4 Sacrificial layers

3.2.4.1 SAC1 and 2

The first PHS-lots prepared showed a very low number of movable pixels. The reason was found in sticking of spring 1 either on the yoke or the baseplate. Besides buckling avoided by passivation of the springs in later lots, one finding of the SEM-analysis was that the upper (SAC2) and lower (SAC1) distance from spring1 to the next metal layers usually is lower than intended and also as measured at in-line measurements on test structures. For PHS#2a, PHS#2b, and PHS#3a one can see in Figure 26, that SAC1 was planned to be 200nm, respectively 220nm, a value hit by the CVD/CMP process on the measured test structures in-line. However, in the MMA we only reached approximately 125nm thickness. Similarly, the result for SAC2, where a target value of 100nm and an in-line measurement of 90nm resulted in only 60nm actual thickness in the MMA.

The main reason is that the test structure is nearly free of any topography, when it is covered by the corresponding USG deposition. The CMP removal rate is then locally close to what is measured on blank wafers. However, in the MMA due to step-like shape of the baseplate and the spring, the deposited USG has significant topography and is removed faster. With less vertical distance, during the release etch it is very likely even with a reasonable bending of the spring to touch the yoke or base plate and stick on them, preventing further movement of the pixel.

Beginning at PHS#4 we tried to increase the sacrificial layer target value as well as shorten the CMP time to an absolute minimum, just enough to planarize the topography inside the MMA. For SAC1, only the shortened CMP increased the actual value from 130nm to 180nm, without any change on the target deposition thickness of 220nm itself. Further increase of SAC1 to 300nm in a second split group further increased the actual value to 260nm. In parallel we tested two split groups for SAC2, 150nm and 200nm target, which got actual values of 95nm and 140nm, a significant increase compared to the 60nm reference value.

In characterization of PHS#4 the number of moving pixels was greatly increased compared to earlier PHS i.e. in the split group with the highest gaps. However, there was a disadvantage, too. Since the yoke has to be connected to the base plate and the hinge, the process flow requires a via patterning at a topography of steep edges on the surface, made by the spring collar. This topography complicates the lithography process i.e. the deposition of the needed anti-reflective coating. As a result, not all vias for the yoke post were opened completely on the wafer, leading to delamination of the actuator during the release.

For PHS#5 as well as the AHS lots, we decided to start with the more secure split group of PHS#4, which was 220nm SAC1 and 150nm SAC2 and gradually increase the value for every lot showing no complications at the via patterning. E.g. for AHS#1a we aimed for 265nm SAC1, actually 230nm and 160nm SAC2, actually 105nm. Together with the second remedy of better passivation described in the next section, this further increased the number of movable pixels compared to PHS#4.

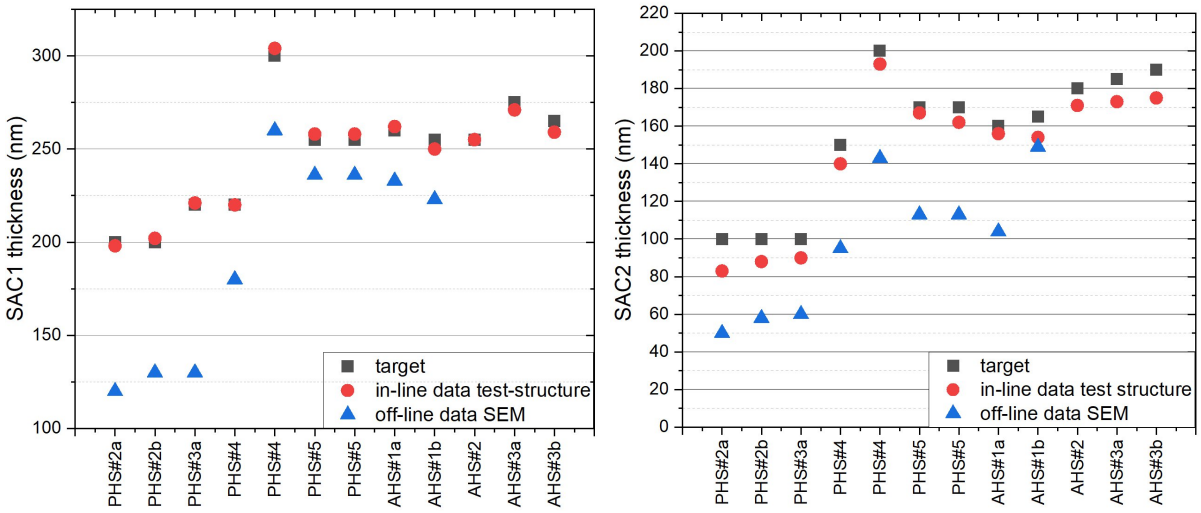


Figure 26: Thickness of sacrificial layer 1 (left) and 2 (right) comparing the targeted values with in-line measures und test structures and off-line data in SEM for all PHS and AHS lots.

3.2.4.2 Vertical gap (SAC3)

One of the parameters defining the final actuator response curve is the vertical gap between the yoke and the stator. It is formed by a USG-layer in a two-step CVD/CMP process already developed and described in former deliverables. Its value is defined in one part by the accuracy of the CVD and CMP for USG. Another part is the Al_2O_3 removal and aSi-filling of the insulating post (see 3.2.5.1), which lower the initial value due to technically necessary over-polish.

Unfortunately, after process development in HTC/PHS, a change in the aSi-CMP process became necessary, due to a change of the polishing slurry. It was decided to do the evaluation of the new slurry on AHS#1a, comparing two different aSi-variants for post-filling, the standard aSi220 and a low boron type called aSi30, which had a better selectivity vs. SiO_2 with the old slurry. The result is shown in Figure 27 (top left). The optimal vertical gap was calculated to be 360nm. On both variants an over-polish occurred, ~10nm for aSi30 and ~20nm for aSi220. The obtained range for a wafer for both variants did not show significant differences, being 10…15nm on all wafers.

A typical distribution of the vertical gap is shown in the bottom right part of Figure 27, with the highest values typically in the north-west corner of the wafer and the lowest in the center and south part. Due to the lower over-polish of aSi30, it was decided to keep this material as standard for the next lots. To compensate the known over-polish, the initially deposited thickness was increased by 10nm. By doing so, for the next lots a stable value close to the target could be achieved as presented for AHS#1b and AHS#2 in Figure 27.

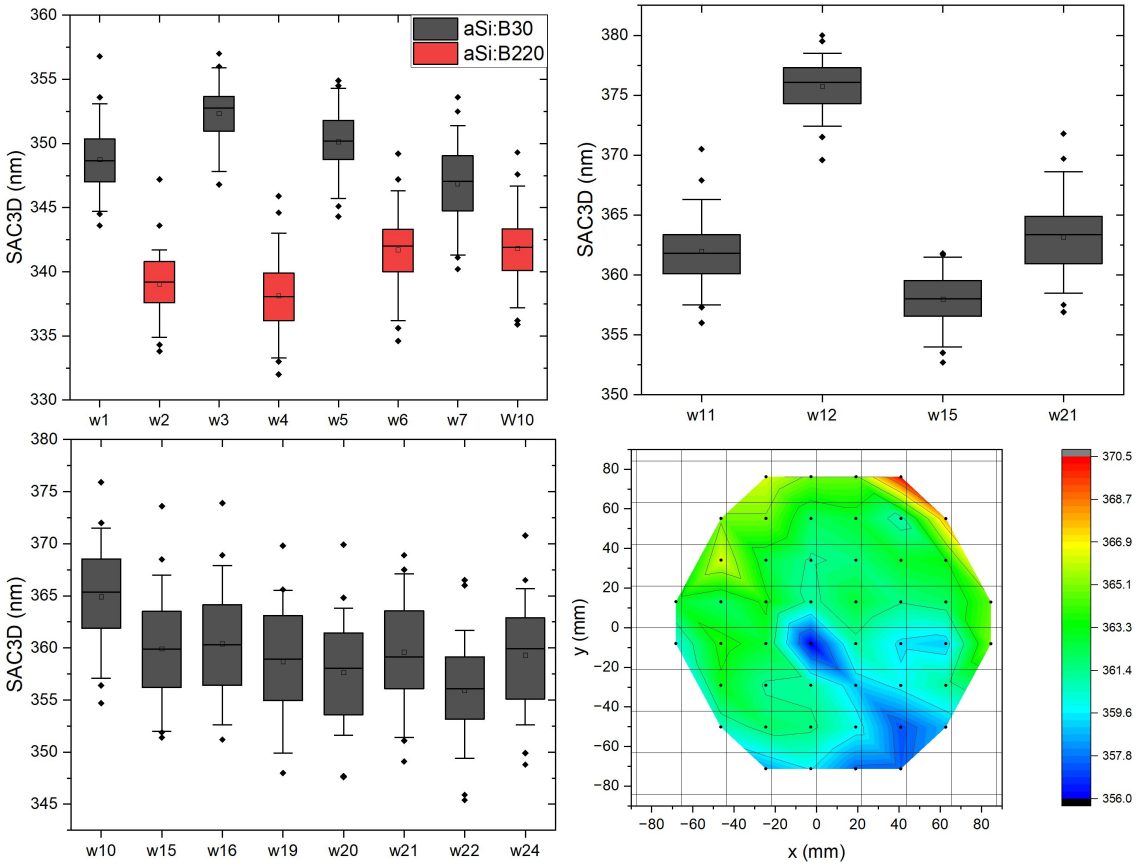


Figure 27: Measured in-line data for the vertical gap (SAC3D) for a target value of 360nm. Top left: AHS#1a, Top right: AHS#1b, Bottom left: AHS#2. For each graph the variation within each wafer is represented by a box plot. Bottom right: representative distribution of the vertical gap on a single wafer (w11, AHS#1b).

Similar to SAC1 and SAC2 (see section 3.2.4.1) we checked possible differences between the in-line measurements on a test structure outside the MMA and the actual value inside the MMA. Again, AHS chips were cleaved in north-south direction, and the cross-section was investigated by SEM. Examples from AHS#1a and AHS#1b are shown in Figure 28. For the investigated chips we observed that the actual values were a little bit smaller than intended, respectively measured in-line. For the AHS#1a chip the in-line measured value at a test structure was 345.4nm, while at the SEM 321.0nm was measured, a difference of 24.5nm. A similar result was obtained on AHS#1b, with 377.1nm (in-line) vs. 353.6nm (SEM), a difference of 23.5nm.

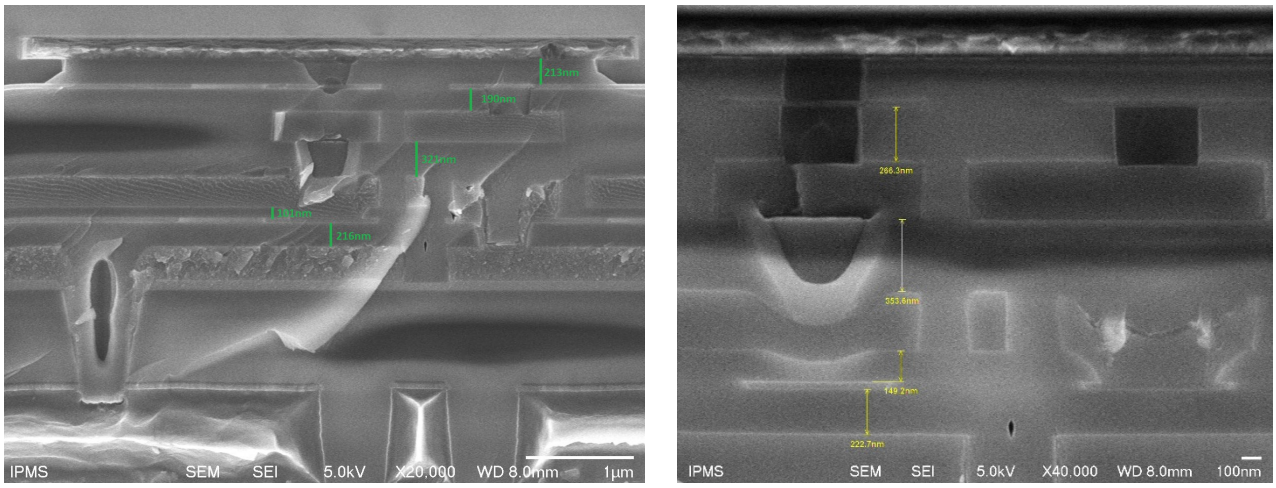


Figure 28: SEM Cross-section in north-south direction of an AHS#1a (left) and AHS#1b-chip (right).

3.2.5 Via filling

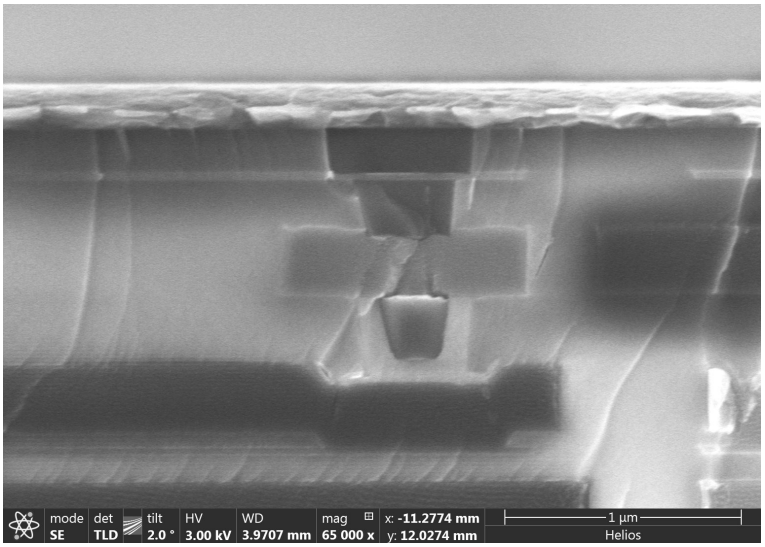


Figure 29: SEM cross-section of PHS#2a showing the mirror post, the spring2 post filled by aSi and the insulating stator post filled by aSi and Al_2O_3.

Another topic needing development was the filling of several vias, i.e. the vias below the mirror, below spring2, and between yoke and stator. The latter has to be insulating inside the active pixel area of the MMA, but outside of this conducting vias are needed to be able to connect the stator to its bond pads. All these vias got new processes compared to former HTC chips, with large improvements of the via quality. In Figure 29 one can see the final result of all three vias stacked.

3.2.5.1 Insulating stator post

To obtain insulation a 100nm thick layer of Al_2O_3 is used, same as already in the HTC process flow. However, the Al_2O_3 back then had been deposited on top of an already planarized via as plate. This led to the issue, that the subsequently deposited stator has some topography with a step-height of approximately the Al_2O_3 thickness. This topography caused some issues at later CMP-processes. Furthermore, such a plate may suffer from bad resist adhesion, when wet etch instead of dry etch is used. To overcome these issues, the sequence of Al_2O_3 and aSi was switched. Now the open via is first filled by 100nm of ALD-Al_2O_3 and subsequently patterned, firstly in RIE and subsequently wet, to minimize overetch into the SiO_2. Then aSi is deposited and planarized by CMP. The result is a fully planarized post with 100nm Al_2O_3 at the bottom and the sidewalls as can be seen in Figure 29. With this process flow, the stator can be deposited without any height variations. As additional benefit, the insulating distance along the Al_2O_3 surface is much longer this way, which should reduce any possible surface leakage currents and thus improve the precision of the addressing voltage and thus actuator position.

3.2.5.2 Spring2- and mirror post

In the HTC and also first PHS lots, the mirror post was only sputter filled. This simplifies the process flows, but lowers the fill factor of the mirror. The new flow uses additional process steps of aSi deposition and CMP with selective stop on SiO_2, to fill the via underneath the mirror without visible voids or steps on the surface, as presented in Figure 29. This is a very large improvement in the optical quality of the pixels, reducing stray light and phase variations.

The second via changed was the one underneath spring2. In former process flows an additional reinforcement, deposited by sputter-PVD, was necessary to fill the via adequately, since the spring itself was too thin. By applying the same process of aSi-CVD/CMP as for the mirror post, the process flow itself could be simplified.

3.2.6 CMOS-Planarity

One of the risks for the AHS lots, which cannot be covered by previous process development is the connection between CMOS and MEMS part. Single process development is done on blank wafers and also HTC and PHS fabrication is done with focus on good planarity of single chips. Using external CMOS fabrication however can result in unforeseen issues and longer fabrication time to compensate poor planarity. To examine the CMOS planarity, it was decided to prepare some wafers without the FEoL part, only the BEoL with 6 metal layers. From this lot it was possible to prepare some remedies for the later AHS lots, without losing additional time for process development. This 6-metal-shortloop was then measured for its topography as shown in Figure 30.

This measurement revealed several inhomogeneities in the height. First and most problematic is that the PCM-frame in the vertical space between two chips lies much lower than the chip itself by several hundreds of nanometer. Such a high step can result in focus and levelling errors during later lithography steps as well as problems during CMP causing local variations in sacrificial layers in the actuator or – as a worst case – a failure of a CMP stop with damage of metal structures.

Based on the early results, a process was developed using additional SiO_2 deposition with subsequent removal in the chip area only. This brings the PCM frame surface to approximately the same level as the chip interior. This process was applied to all the AHS lots. The result for AHS#1a is shown in Figure 31. There is no substantial height difference between PCM and the chip, as desired.

However, the surface shape already visible in Figure 30 now becomes clearer to be observed. On a first glance the surface looks like a parabolic bowl-like shape, with height differences of approximately 700nm from chip center to the edges. Extracting a curvature from the data still reveals some random roughness in y-direction and – more critical – a higher order deformation in x-direction as also visible in Figure 31. A parabolic component of the shape can be compensated in the optical system for the final device, while significant amounts of higher order deformations cannot. For AHS#1a we decided to continue processing without further planarization to not delay a first wafer-out further, while AHS#1b and later got some extra planarization processing to reduce the higher order deformations mentioned above.

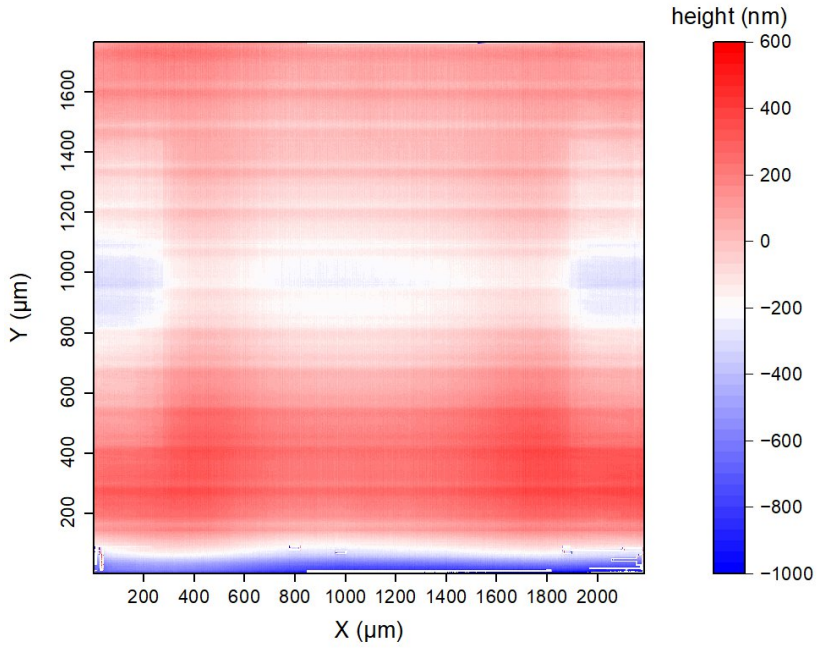


Figure 30: Profilometer scan of the 6-metal-shortloop after delivery to Fraunhofer IPMS. The deep blue area at the bottom of the image is the PCM frame.

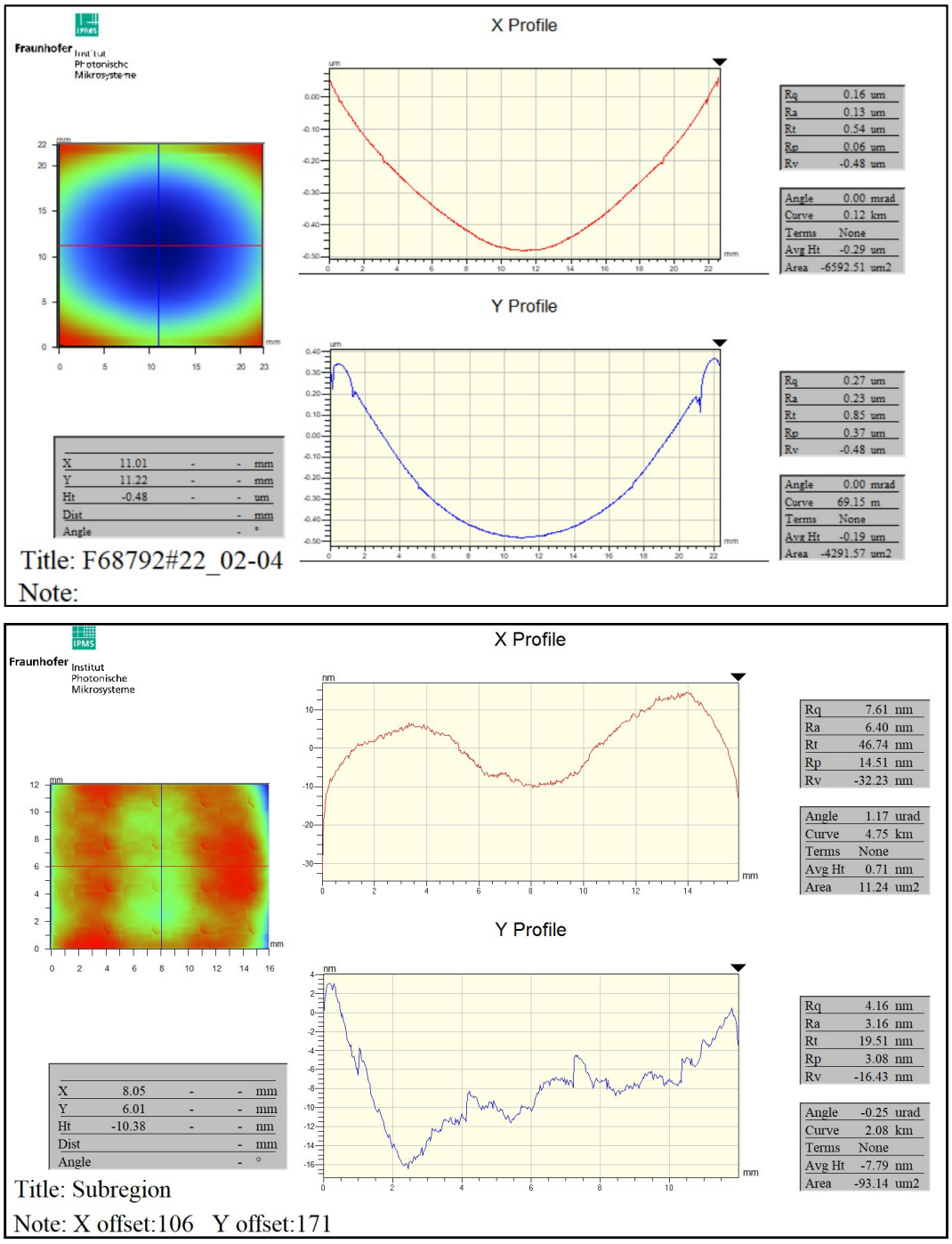


Figure 31: WLI-measurement of a complete chip surface after planarization of the PCM-frame for AHS#1b. Top: Only tilt subtracted. Bottom: Tilit and curvature subtracted for the MMA area.

Since even with compensation of the CMOS planarity, the bowl shape with several hundreds of nanometer height difference remains on all the chips, as it cannot be compensated without more complex processes. For the AHS extensive use of DUV lithography is made. It allows finer feature sizes but at the cost of lower depth of focus. For simple structures like vias or the springs, this did not matter. However, for the yoke with narrow fingers and the cross-talk ring, which required thicker resist, it turned out that the parameter setting developed on PHS could not be applied on AHS. As presented in Figure 32 the first trial with best settings from PHS, the height difference between the MMA center and the edge was higher than the depth of focus, causing a collapse of the resist at the edge, while in the center the resist looked quite good.

To overcome this problem a rework with a defocus was necessary. The result of that rework in resist as well as after patterning is shown in Figure 33. By shifting the focus, we could avoid the collapse

of the resist, which is the most important point, but for the price that the fingers lose some pattern fidelity since they are now too far from optimal exposure settings. This is unfortunately a necessary trade-off at this time. The situation could be improved by optimising the process flow further in a possible follow-up project. Fortunately, the bad resolution in the resist does not fully transfer into the etched pattern of the fingers, thus their length and corner rounding are still similar over the full MMA area. However, a small influence on the finger width cannot be fully avoided resulting in a worse CD-uniformity than the one obtained from the PHS lots. This will translate into some variation of response curve parameters across the pixel area of an MMA chip, which then needs to be corrected by modified addressing data according to calibration.

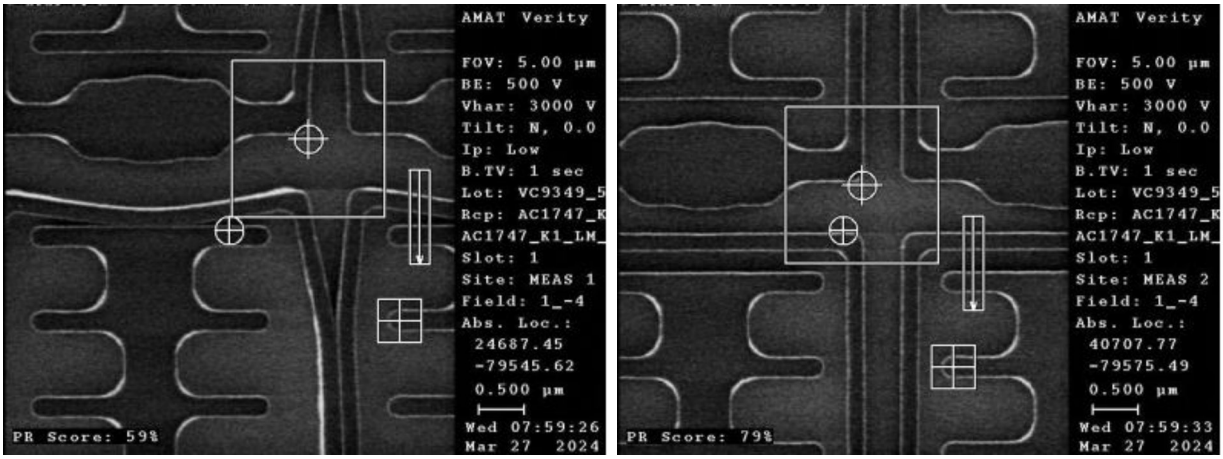
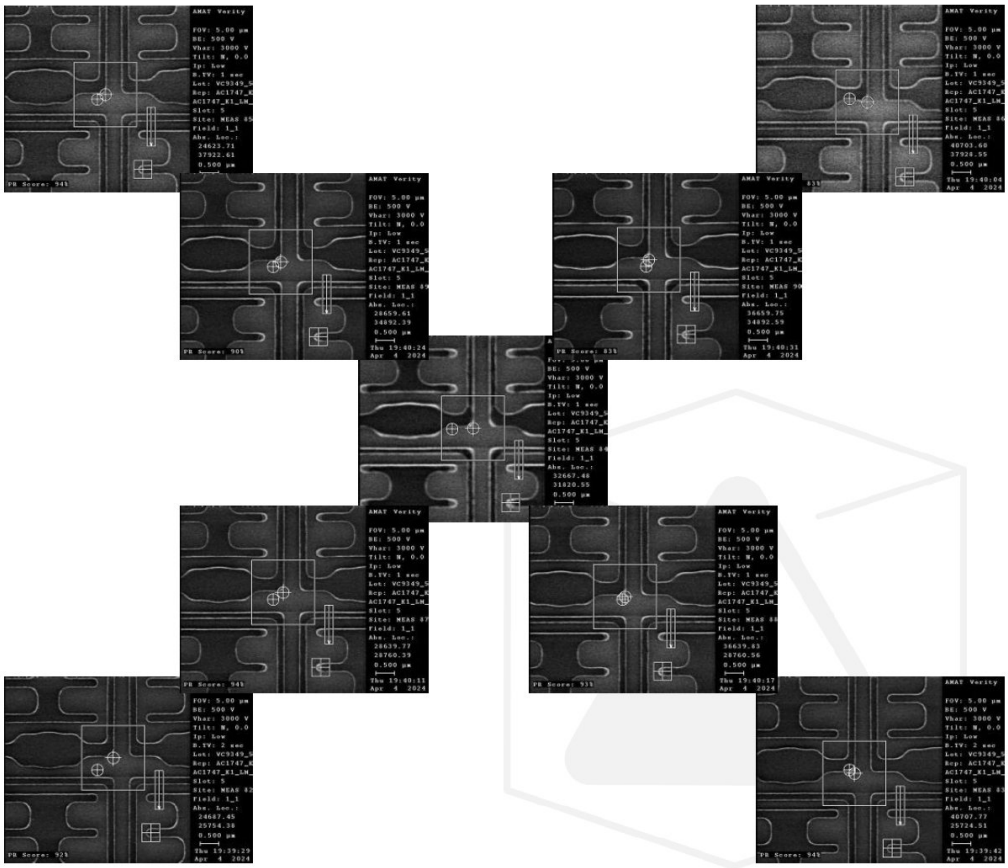


Figure 32: CD-SEM top view of the resist mask for the yoke in AHS#1a for the first exposure trial at the MMA edge (left) and the MMA center (right). Due to focus errors caused by the chip topography, the resist collapses at the edge.



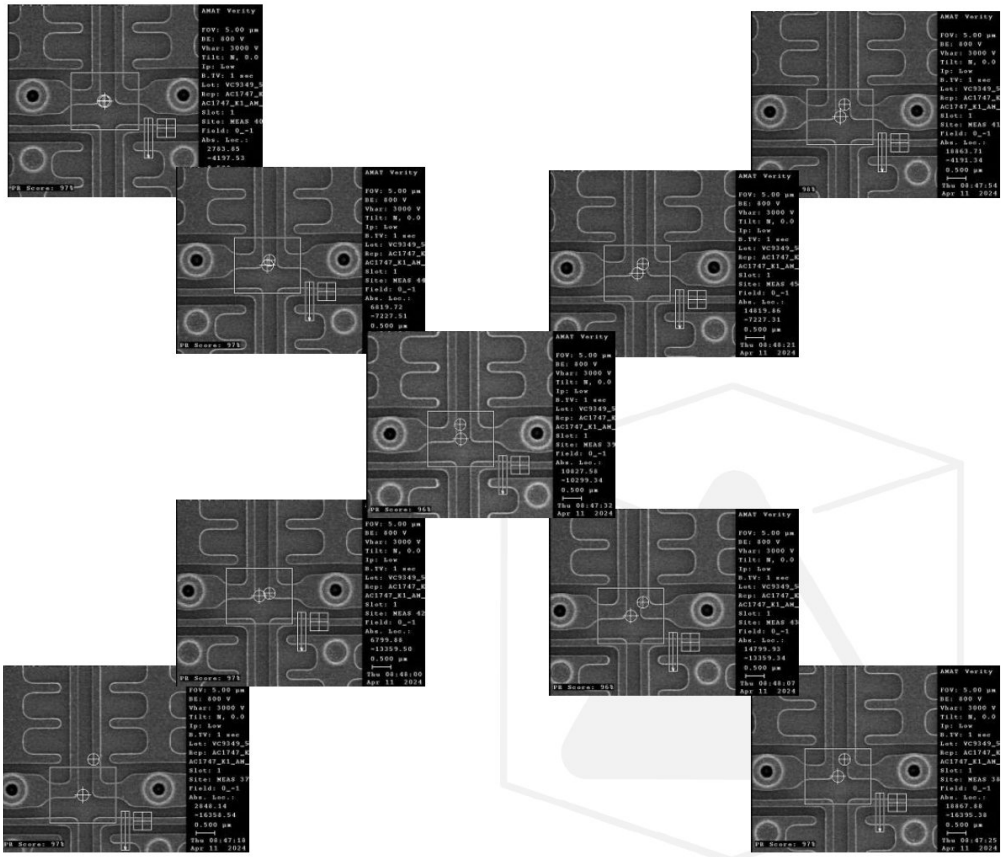


Figure 33: CD-SEM top views of the resist mask (top) and after patterning (bottom) for the yoke in AHS#1a for the second exposure with focus offset. The image arrangement represents the measurement position on the MMA, corner, half diagonal and center.

3.3 Chip processing

3.3.1 Release

The standard process flow after wafer dicing includes removal of the sacrificial layer material followed by visual inspection (Figure 34) and WLI measurements (Figure 35). While the first one allows qualitative comparison of chips and processes, looking for delamination, scratches etc. the later one is a quantitative analysis for pre-deflection in 3 dimensions (z-shift, x- and y-tilt) as well as planarity of the mirror. Both provide the information to select the best chips qualifying for final packaging, testing and delivery.

The WLI-measurements include 13 measurement points arranged over the full MMA as shown in Figure 35, with a total of ~5500 pixels measured. This data is further analyzed for statistics of pre-deflection like in the histograms of Figure 36. Relevant for the tilt-modes is a low mean value of at max <0.2°, better <0.1°, as well as a low standard deviation. The initial mean value of the piston mode cannot be evaluated due to the lack of reference pixels, thus only the standard deviation is analyzed.

For all three parameters the standard deviation is determined by two effects, sticking pixels as discussed on one hand and on the other hand residues remaining after the release process. Usually, the three parameters of pre-deflection show a behavior closely to a normal distribution. A higher amount of residues cause a widening of the distribution curve, but without significantly deforming it. Sticking pixels however have a significantly lower height than the mean and are usually also tilted heavily. Thus, they can be identified as single counts or in higher amount as second peak in the histograms. In Figure 35 there are 4 sticking pixels (blue) in the south-west corner significantly lower

than the other pixels. In Figure 36 these pixels can be recognized as 4 single counts in the range of -60...-80nm.

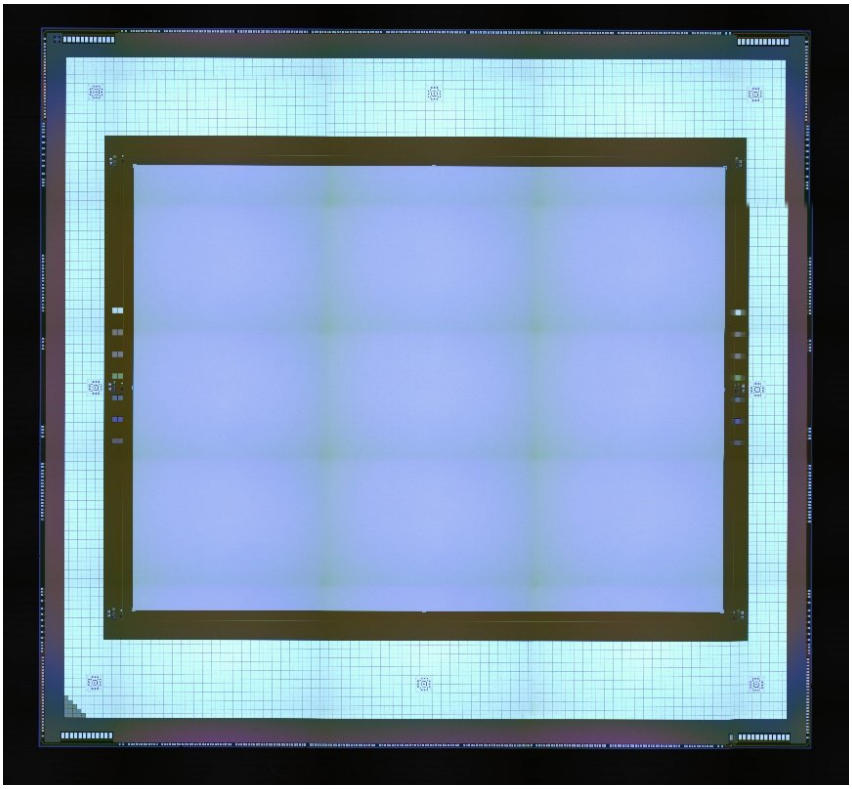


Figure 34: Die-Shot of an AHS#1a chip after release. The darker vertical and horizontal lines are caused by non-uniform illumination and image stitching, but not actually there on the chip.

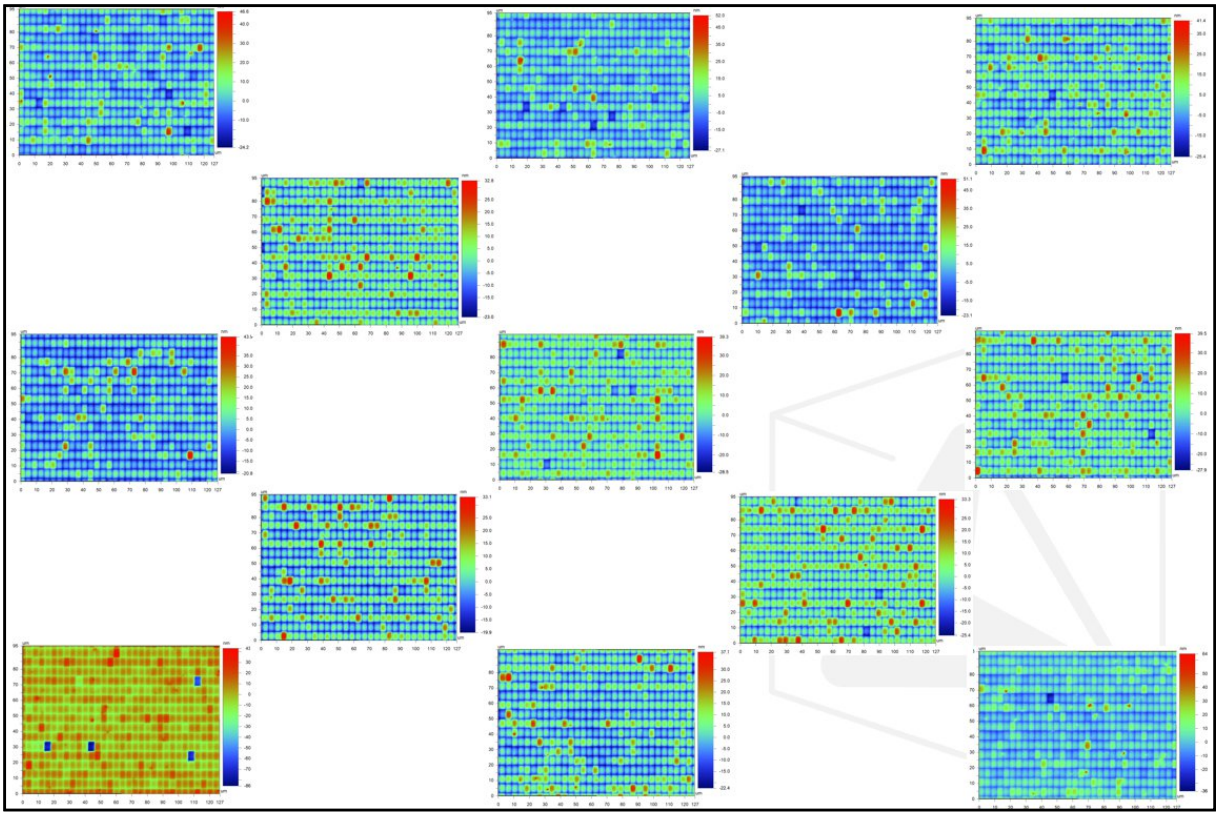


Figure 35: WLI height data for 13 measurement points of an AHS#1a chip taken after release. The image arrangement reflects the actual distribution of the measurement areas on the chip.

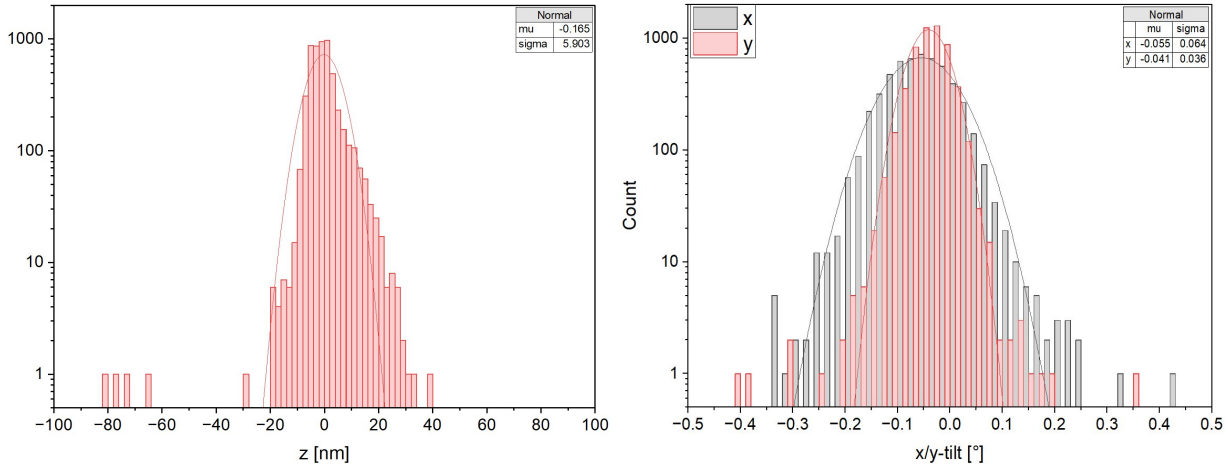


Figure 36: Histograms of the data presented in Figure 35 for the vertical pre-deflection (left) and both tilt directions (right).

3.3.2 Post-Release Cleaning

The values obtained for spread of pre-deflection, mostly in z-direction, were not satisfying at the beginning. Different releases or combinations of them were tested with the goal to get the most aggressive release etch for removing restraints but soft enough to not induce additional stress to the hinges. The provisional approach was a short CF4/O2-plasma (CDE) combined with a medium HF vapor release. To further improve the uniformity of pre-deflection, we tested two approaches for a post-release treatment. The first one was a 24h our treatment in humid air, followed by an additional cycle of low HF vapor. This approach was successful at least on the inner 90% of the MMA, but is a less defined process. Later we used an H_2-plasma in optional combination with HF vapor. As shown in Figure 37 the spread mostly in z- but also x- and y-direction could be reduced by this treatment. Finally, a reduction of on average 15% of the 3sigma value in z-direction could be obtained by H2-plasma only. An additional HF treatment is optional, and a benefit heavily depends on the initial value of pre-deflection spread (Figure 38).

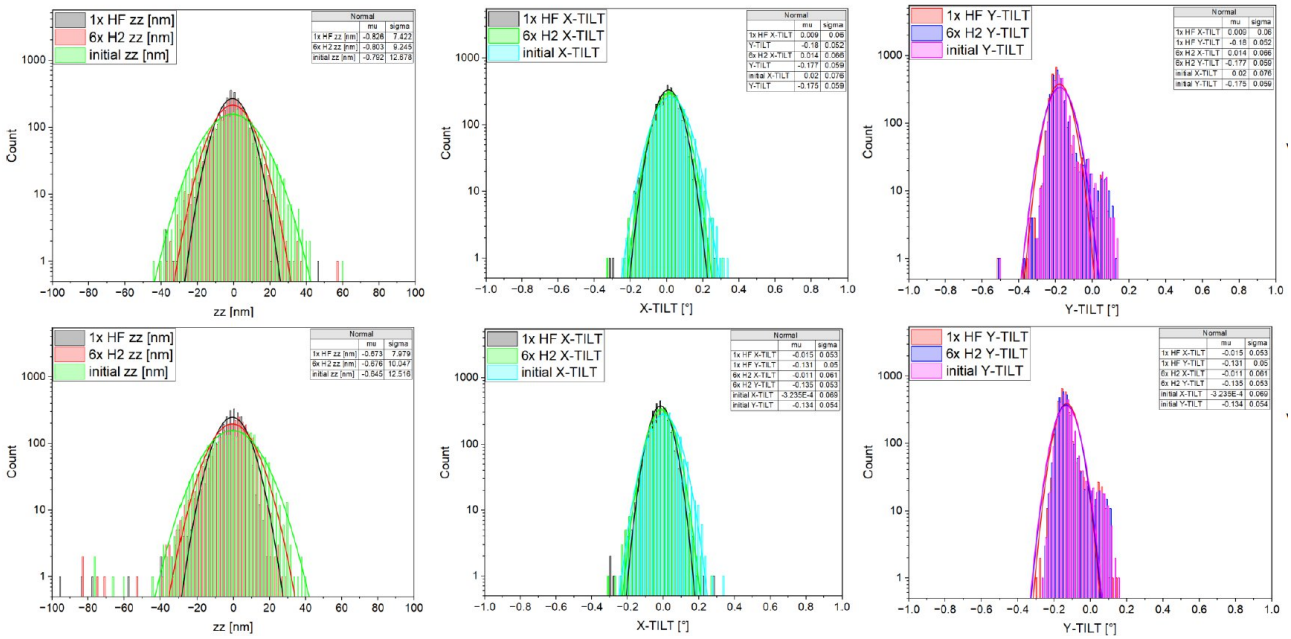


Figure 37: Histograms of 2 chips showing the change in predeflection by a post release treatment of H2 plasma and HF. Left: z- direction, center: x-direction. Right: y-direction.

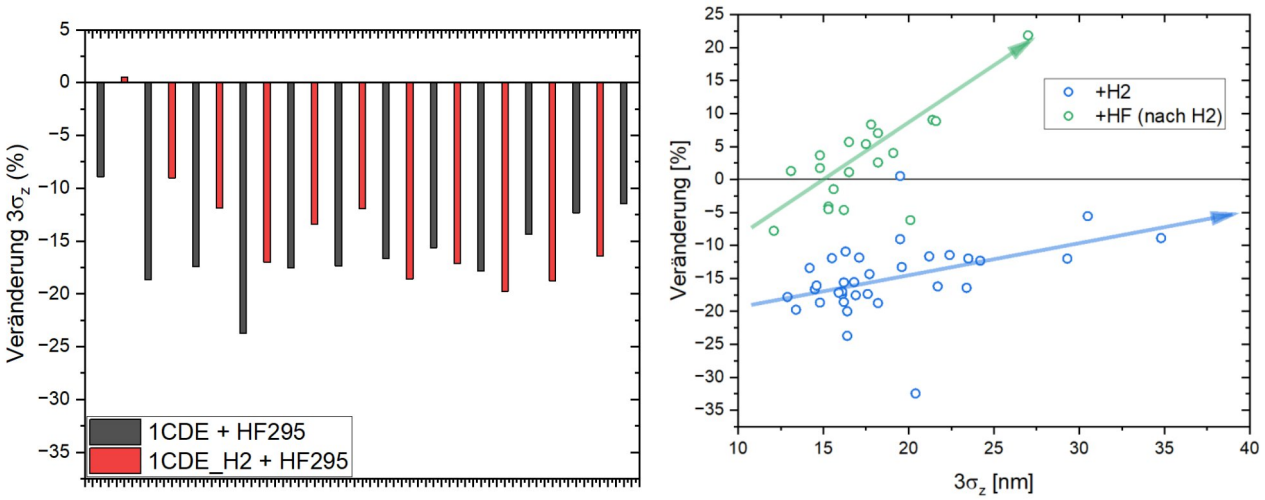


Figure 38: Left: Change of standard deviation of the pre-deflection in z-direction for a batch of AHS-chips after H_2-plasma. Right: Change of standard deviation of the pre-deflection in z-direction for the same chips after H_2-plasma and subsequent HF-process vs. standard deviation of pre-deflection initially after release.

Using the best combination of spring passivation in the wafer process and combining it with the current approach of release and post-release treatment, a 3sigma-value of 10nm could be reached for 36nm thick springs and 15nm for 32nm spring thickness, respectively. However, process development for both passivation and release/post-release is still in progress and we see big potential and need to further improve the uniformity of pre-deflection.

Chapter 4 MMA Chip Packaging

4.1 Packaging Concept

A micro mirror array with active backplane is in many respects similar to other electronic circuits. The packaging, however, has not only the usual requirements, but quite a few more:

- Electrical interface (challenging)
  - 144 digital high-speed differential data inputs with very low error rate
  - high-precision supply and analog reference voltages for the DACs
- Cooling (average requirements)
- Mechanical protection of MMA and backplane (challenging)
  - micro mirrors are extremely sensitive to any mechanical contact
  - keep of dust and organic or corrosive contaminants, no cleaning possible
  - keep out moisture to avoid corrosion (no passivation) and sticking
- Optical interface (challenging)
  - global planarity of MMA needs to be very good and stable for the whole lifetime
  - window with low reflection, low distortion, and high transparency in the visible range
- All packaging processes need to be as close to room temperature as possible (unusual)

To meet all these requirements, we developed the packaging concept in Figure 39.

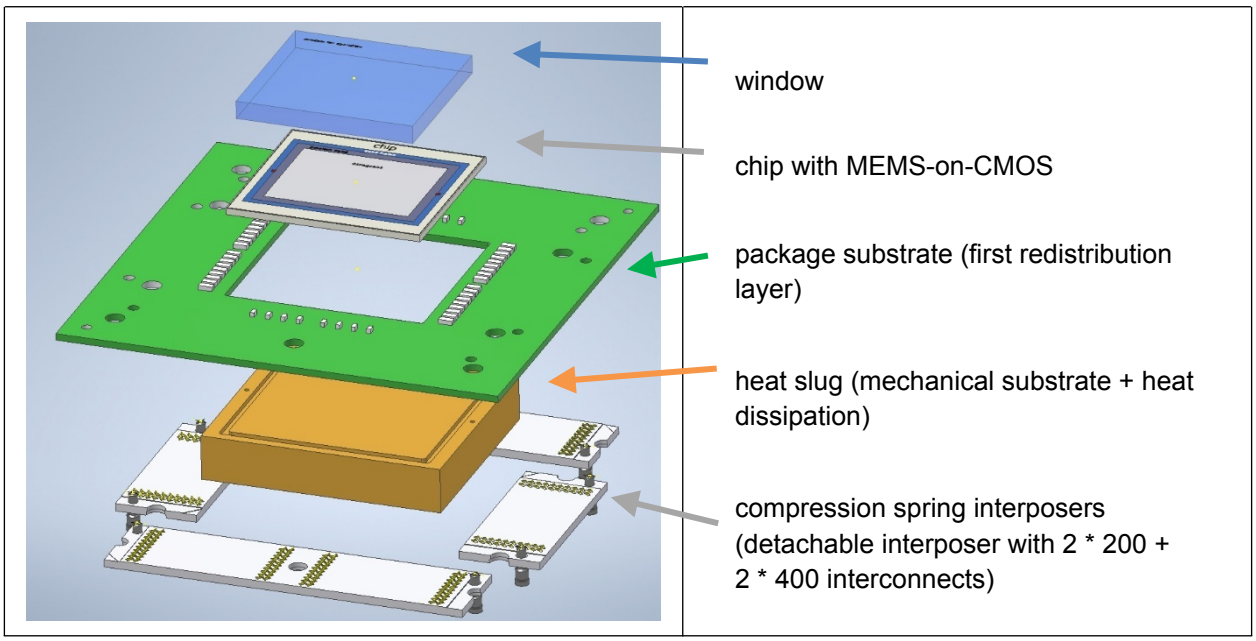


Figure 39: REALHOLO – first level package: AHS chip module with compression spring array interposers

4.2 MMA Packaging

4.2.1 Assembly of the chip module - first level package

The first step during assembly of the chip module is the attachment of the so-called heat slug. The attachment of a block of metal onto a PCB sounds simple but holds some challenges when precision is required. Adhesive bonding of both parts happens within a narrow frame of <1 mm. On both mating parts it must be ensured that the adhesive is not entering into neighbouring regions, to avoid contamination of the chip die-bond zone or the land grid arrays on substrate back side. With a careful choice of the used epoxy and the applied dispensing parameters Fraunhofer IPMS managed to solve that issue.

During assembly and later operation, the module will be exposed to temperatures between -20 C … +125 °C. To reach a reliable bond under those conditions, the management of the CTE-mismatch is an important topic. CTE mismatch of the involved materials needs to be small enough and the adhesive bonding should be rather flexible. Otherwise, the CTE-introduced stress will cause delamination after some cycles of heating and down cooling. Below you find a depiction of the geometrical circumstances during assembly (Figure 40).

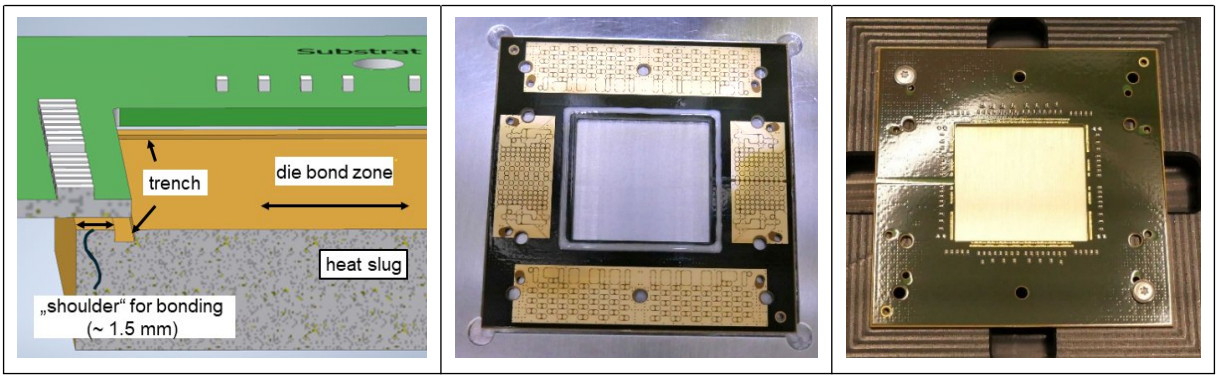


Figure 40: Assembly of pre-module, attachment of heat slug on substrate: (a) design details, (b) view on package substrate after adhesive deposition, (c) front view of pre-module

The next step of the chip module assembly is the die bonding. Dispensing of the die-bond adhesive is less critical compared to other assembly steps since position and volume of the adhesive trace doesn't need to be very precise. However, placement of the MEMS chip with its minimum pad pitch of 70 µm requires a certain accuracy to align the chip bond pads to those of the package substrate. The later step of fine-pitch wire bonding requires a lateral placement accuracy from chip to substrate of less than half of the pad pitch (< 35µm) and an alignment of the chip bond pads of 10 µm…30 µm above the substrate pads.

All micro-assembly steps within the presented work were carried out using an advanced die bonder. Parallel to the basic tool further equipment had to be designed to enable such a complex multi-step assembly process with lateral placement accuracy of a few micron. Fraunhofer IPMS designed e.g. component trays to supply the parts in an appropriate manner on the machine table or mounting stages to hold the components in position during assembly. For pick and place of the sensitive MEMS chip Fraunhofer IPMS designed a vacuum bond head together with the tool supplier that touches the chip only within a narrow area between the active pixels and the bond pads.

Micro-assembly tasks depend in general on the successful position detection of all components on the machine table. The challenge is a precise recognition of a component body edge or a dedicated fiducial mark by the pattern recognition software. The following figures show examples of different

components, which are involved in the process and their individual structures for optical recognition. Figure 41 shows the bond tool used for MEMS-chip pick and place. On its front side there are eight contact zones (width < 1 mm) to touch and hold the chip and separate drill holes for optical recognition by the bonder. Further down you find depictions of substrate and MEMS chip with their structures for identification. The recognition of the substrate works by a set of individually shaped bond pads, see Figure 42. The identification of the MEMS-chip uses two groups with vernier scales and other geometries that extra have been processed as part of the MEMS top-metal layer (Figure 43).

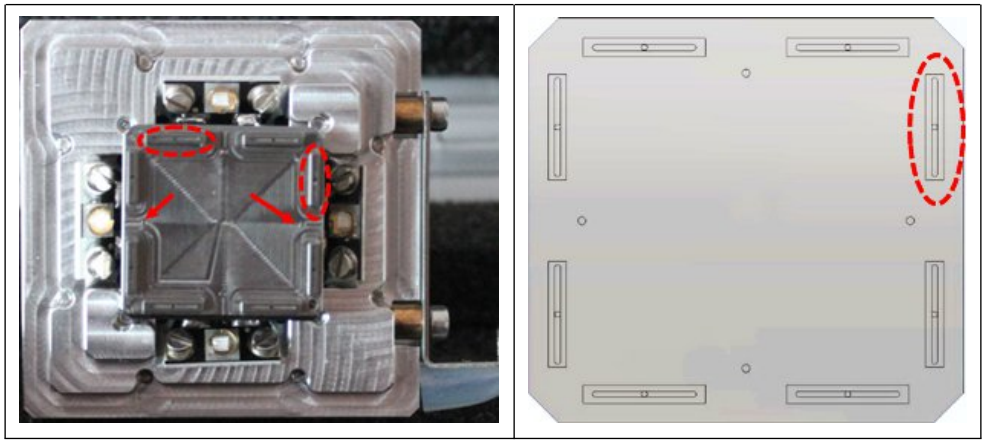


Figure 41: Bond tool for chip pick and place: (a) front view of bond head and surrounding mechanics, (b) detailed view on channels and contact zones to MMA chip

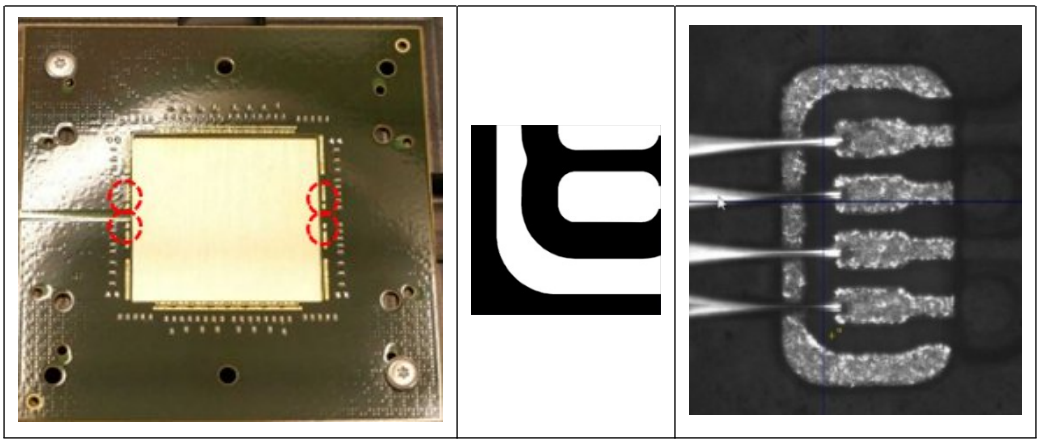


Figure 42: Fiducial marks on package substrate used for position detection: (a) position of fiducial marks on substrate; (b) provided pattern for alignment by detection software, (c) real structure on substrate, detected by bonder

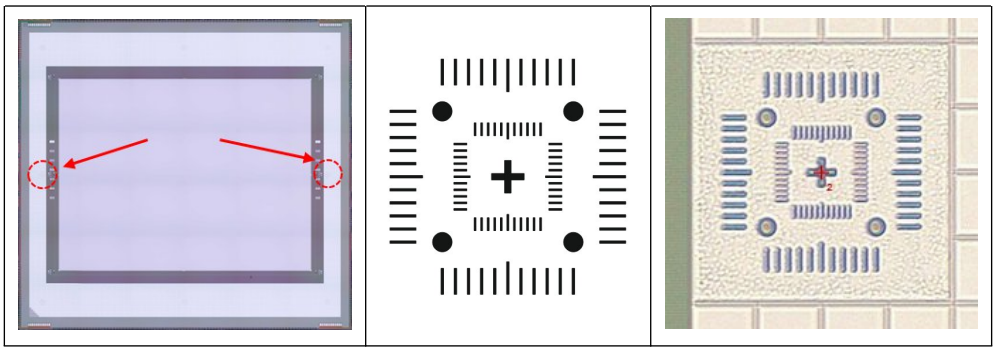


Figure 43: Fiducial marks on active chips for optical position detection for die bonding: (a) position of fiducial marks on chip; (b) provided fiducial mark in software; (c) real structure in chip, detected by bonder

First runs showed a situation where the chip was placed shifted sideways and rotated into one of the corners of the PCB pocket with a misalignment larger than 100 µm, which is huge compared to the bonder's real capabilities. Even if the wire bonder would be able to compensate such a misalignment the consequence would be to end up with different length of the bond wires on opponent chip sides and a higher risk for short cuts between neighbours of the staggered loops. It turned out that the recognition of the substrate position has not been precise enough. After fixing that, Fraunhofer IPMS managed to obtain the chip placement in an appropriate accuracy of +/- 20 µm, to less than half of the pad pitch (Figure 44).

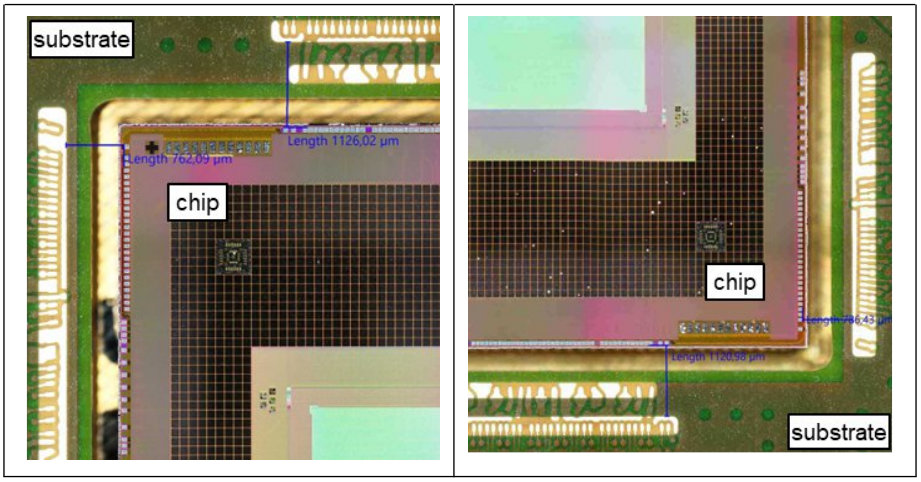


Figure 44: Die-bonded chip with appropriate lateral alignment accuracy: (a) NW chip corner, (b) SE chip corner

After further testing, Fraunhofer IPMS also found a promising combination of deposited adhesive volume and added glass beads to ensure the precise control of chip height level, which is also required for the following wire bond step. Placement of the chip happens force-controlled to ensure a direct contact to the underlying glass beads and to prevent the chip from floating on top of the adhesive and from drifting aside.

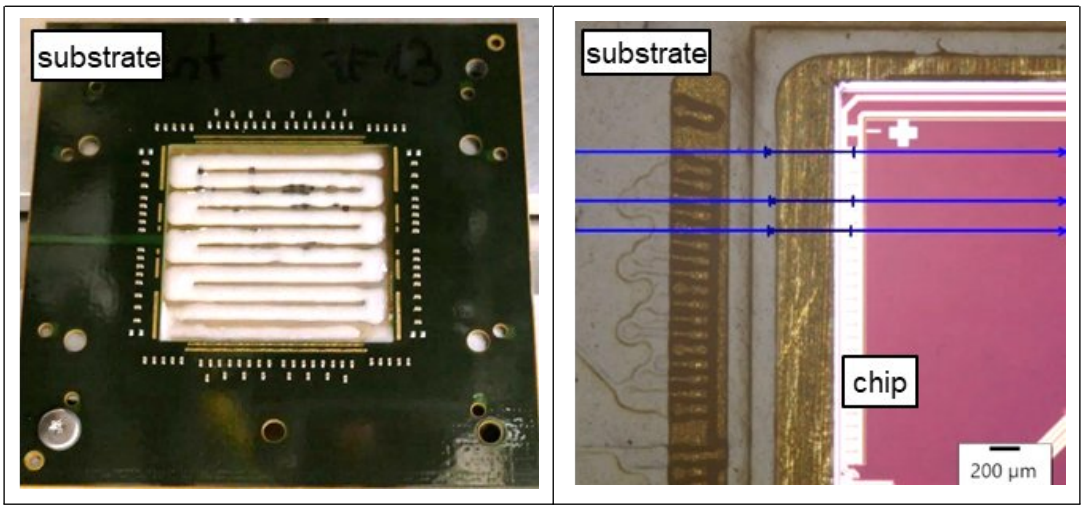


Figure 45: Verification of chip height level with respect to surrounding substrate bond pads: (a) dispensing of die bond adhesive with glass beads (b) measurement of bond pad height level after chip placement

4.2.2 First-level interconnect – fine pitch Al wire bonding

First-level electrical interconnect from chip to package substrate is carried-out via wire bonding technology. Wire bonding is well established for MEMS electrical interconnects, even for pad pitches below 100 µm. For power and signal distribution, more than 700 fine-pitch aluminum bond loops are connecting the MEMS chip to the substrate. The bond pads of the chip are distributed along all edges of the die to allow the shortest loop length to the substrate. The standard technology for MMA fine-pitch wire bonding used at Fraunhofer IPMS is ultrasonic bonding with aluminium wires of 20 µm/ 25 µm. The configuration has the advantage of a process at room temperature and a certain robustness against minor pad contaminations. Ultrasonic bonding only uses the ultrasonic energy to scrub and deform the wire-to-pad interface. The configuration helps to break through thin layers of surface contaminations or oxides and to expose clean metal surfaces for bonding. In Figure 19 below you see the bond map with the chip in the central opening of the substrate and more than 700 bond loops along the chip edges.

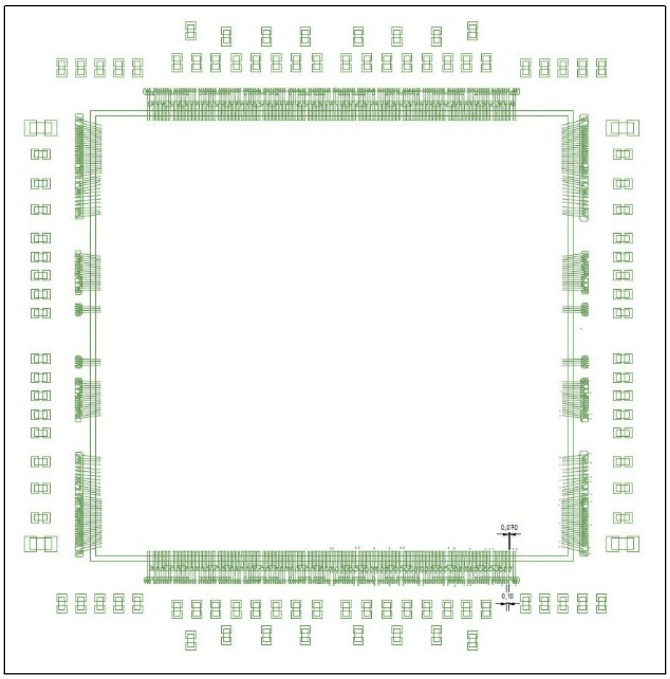


Figure 46: Bond map with the chip in the central opening of the substrate (PCB) and more than 700 bond loops along the chip edges

The applied process with 25 µm Al wire wedge-wedge bonding, forms a wedge on both components into the pad metallisation. Below (Figure 47) you find a detailed view of bond loops from different chip sections. Within the pad areas from substrate north and south side, the bond pads were arranged staggered to expand the narrow pad density a bit (a), (c). Some of the loops from the inner pad row are running slightly inclined to meet the target pad on chip side. From this follows a certain risk for shorts between these loops and neighboured loops from the outer pad row. This is why the chip placement with respect to the surrounding PCB had to be so precise, with a lateral misalignment of less than half of the pad pitch.

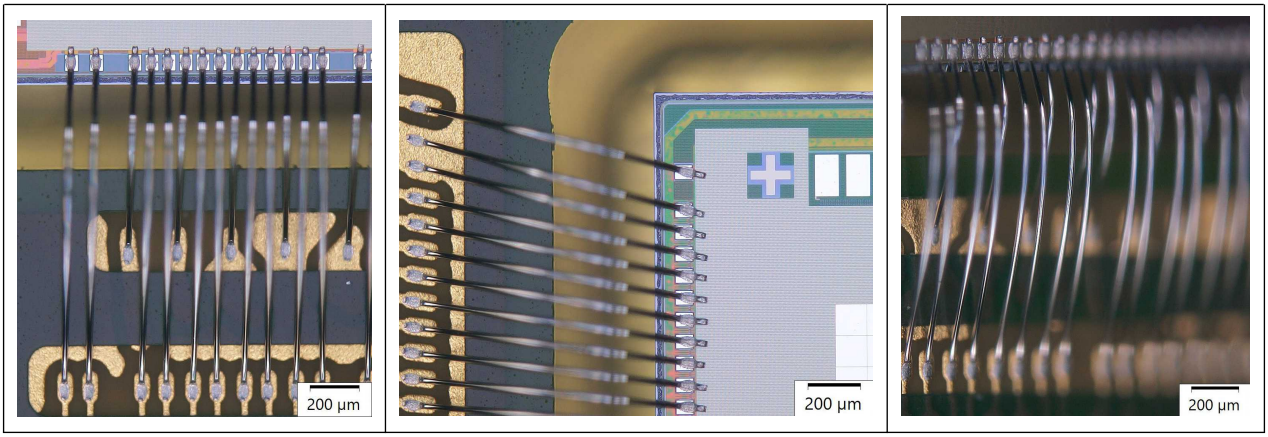


Figure 47: Detailed view of bond loops: (a) loops with staggered pads from chip SW corner, (b) loops from chip NW corner, (c) loops from staggered pads in chips SW corner, observed in a tilted mode

Figure 48 below shows stitched images of completely wire bonded devices. In (a) you see a CMOS chip without the MEMS and mirrors on top. Some of these chips were packaged and contacted to have them available for the isolated characterization of the CMOS backplane. In (b) you find the final AHS device with MEMS on CMOS. The high-reflective mirror array is clearly visible.

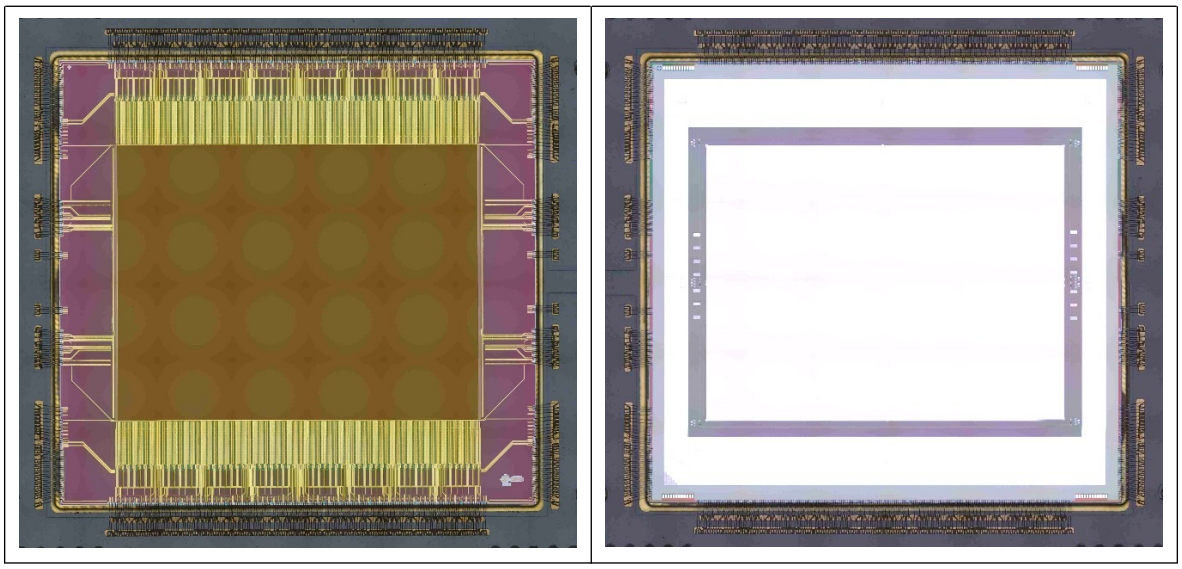


Figure 48: Stitched images of complete devices after wire boding with 25 µm Al wire wedge-wedge bonding; (a) CMOS-chip (no MEMS on top) for CMOS characterization, (b) final AHS chip (MEMS on CMOS)

4.2.3 Mechanical integration of chip module + control electronics

The integration of the first level package, with chip and package substrate, together with the control electronics under the consideration of various mechanical and electrical aspects requires an appropriate mechanical setup, which we call the “inner mount”. The design of the inner mount was an iterative process together with the partners to meet all technological aspects. The inner mount brings all the components together, integrates the MEMS chip with data/ power PCB and ensures heat dissipation.

The core task of the inner mount is the 2nd-level interconnect with a detachable interface between package substrate and data PCB. The solution was the usage of four separate compression spring array interposers which allow a low-profile and high-density board to substrate connection of up to

1,200 contacts. The critical points of the design considerations were the required precision and the robustness to ensure a reliable and easily accessible procedure for a frequent exchange of the chip module. The lateral alignment of interposers and both mating PCBs is ensured using several precision alignment pins and a well elaborated dimensioning of the drill hole pattern in both PCBs.

The compression of all the springs requires a total compression force of 300 N. For homogeneous compression and to avoid local over-pressurization of the PCBs, two separate stiffener plates for top and bottom side of the PCBs were designed.

Figure 49 below shows the exploded view of the inner mount together with the chip module (MEMS chip, heat slug, package substrate), the control electronics (data and power PCB) the compression spring interposers and further mechanical parts for thermal management and integration into the system demonstrator.

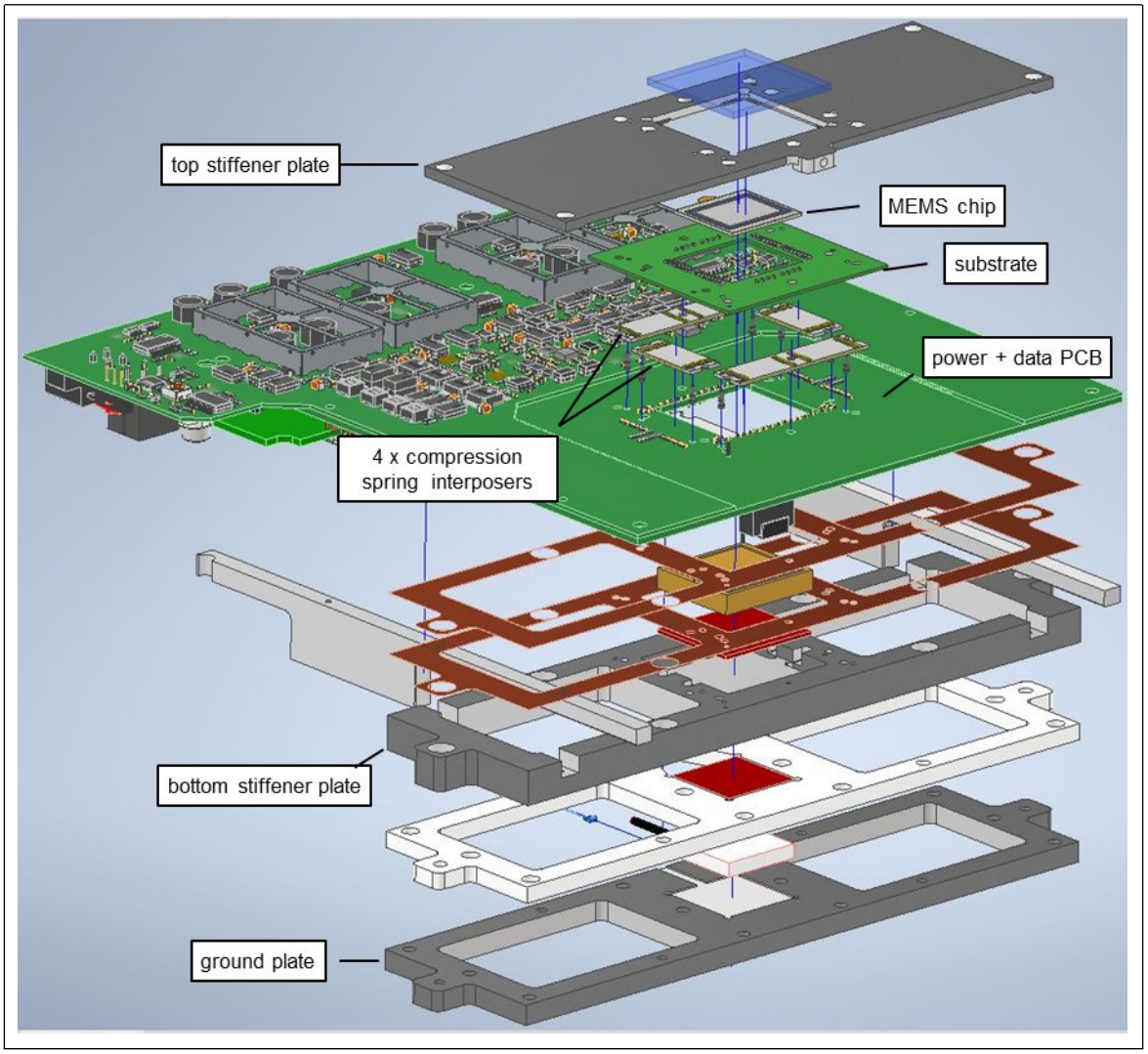


Figure 49: Exploded view of the inner mount together with chip module, compression spring interposers and control electronics (data/ power PCB)

A detailed view of the underlying data PCB with its central opening for the heat slug, the surrounding four LGAs, each for one interposer, the drill hole pattern for the alignment pins and fixtures is depicted in Figure 50 (a) blow. Figure 50 (b) shows the same detail of data PCB, including the four mounted interposers

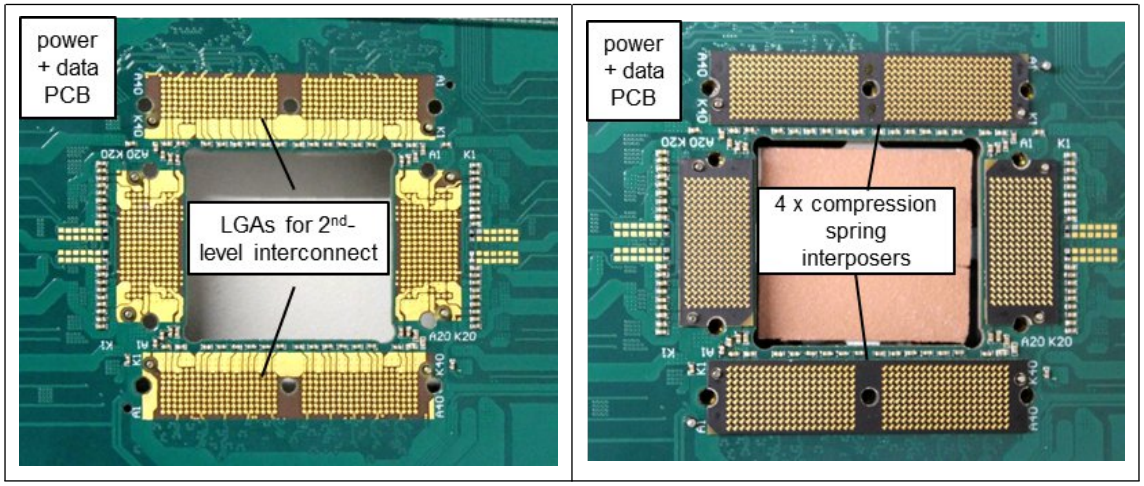


Figure 50: Detailed view of data PCB (top side) with its central opening four LGAs and alignment pins, (b) mounted compression spring array interposers on alignment pins

The AHS-operation dissipates 2 W … 5 W. A thermal output in that order of magnitude requires a concept for heat transfer towards a defined heat sink and the control of chip temperature to avoid overheating and damage. For that purpose, the setup holds a Peltier element on top of the ground plate and two thermal sensors on the Peltier's cold and hot side (see Figure 51). The Peltier top side provides a defined temperature and acts as heat pump to guide the AHS thermal losses into the underlying ground plate and a water-cooled chiller. For assumed thermal losses of 1 W…5 W, there is a temperature difference between chip and Peltier cold side of 1.4 K … 7 K caused by thermal conduction in the intermediate parts. That thermal gap has to be considered for driving the Peltier and for AHS temperature control.

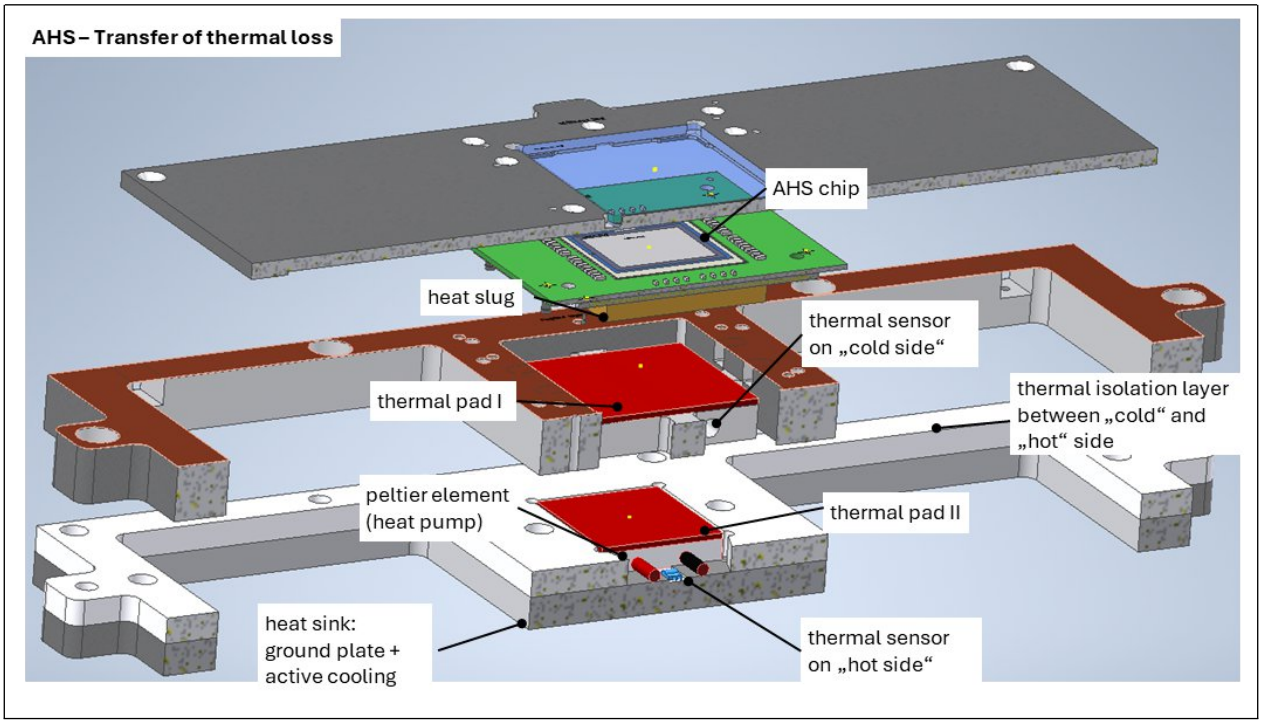


Figure 51: AHS-Transfer of thermal losses from AHS chip to heat sink

4.2.4 High precision window assembly

MEMS micromirrors have to be treated very carefully during their operation and also during their storage. Micro actuators have to be protected against dust and humidity and cannot be exposed to normal air. Accordingly, is the encapsulation of MEMS devices a standard procedure to extend their lifetime and sometimes even to enable an operation as such. Operation of the AHS also requires the usage of a protection window, which, in the present case, needs to be attached directly on top of the MEMS chip.

Bonding of the window onto the chip is supposed to happen within a narrow frame of less than 500 µm width within the area of the passive structures, that are surrounding the active matrix. Here, between the active mirrors and the bond pads, is the only section of the chip where the physical contact is not directly causing damage on underlying functional structures. Nevertheless, since the top metal layer of the active matrix and of the surrounding passive structures are of equal height, a gap of a couple of micron needs to be ensured between window and chip surface (see Figure 52).

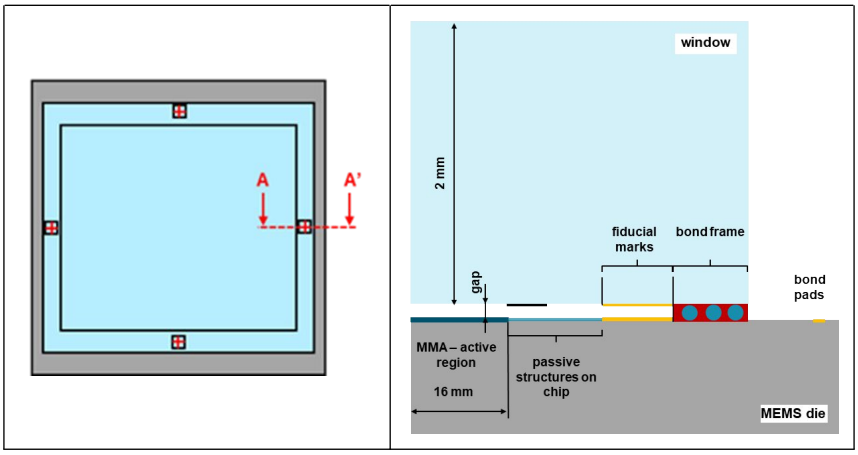


Figure 52: Drawing of window on MEMS chip: (a) position of different sub-sections with fiducial marks, (b) cross section of bond region along the outer edges of window and chip

The risk for contamination of neighbouring structures by the deposited adhesive requires a precise control of adhesive position and deposited volume. For that purpose, Fraunhofer IPMS has carried out extensive pre-tests on that topic. For the optimization of the deposition process precision nozzles with inner diameter of 50 µm...100 µm and a varying amount of the used glass beads have been tested. Finally, Fraunhofer IPMS succeeded to generate epoxy lines reliably with a line width around 150 µm (see Figure 53).

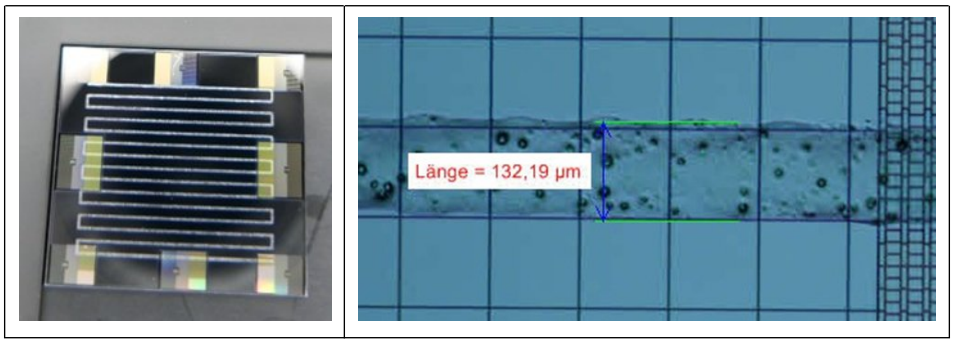


Figure 53: Process development for adhesive deposition: (a) test chip with deposited adhesive lines, (b) detailed view of deposited adhesive line including the 8 µm glass beads

For window pick and place Fraunhofer IPMS also used its advanced die bonder. All the required product related hardware like the customized bond tool, component trays or mounting stages were designed in an early project phase. In Figure 54 (below) you see a picture showing the vacuum mounting stage that holds the chip and the window attached on top.

A precise localization of window and chip is enabled by use of high-precision alignment marks on both mating partners. Marks on the window lower side were processed in Cr. The fiducial marks on the MEMS chip were processed together with the micro actuators and are situated in the same layer as the mirrors. The alignment marks allow the detection of components by the image recognition software and the evaluation of reached precision after assembly. Their layout and position is described in the Figure 55.

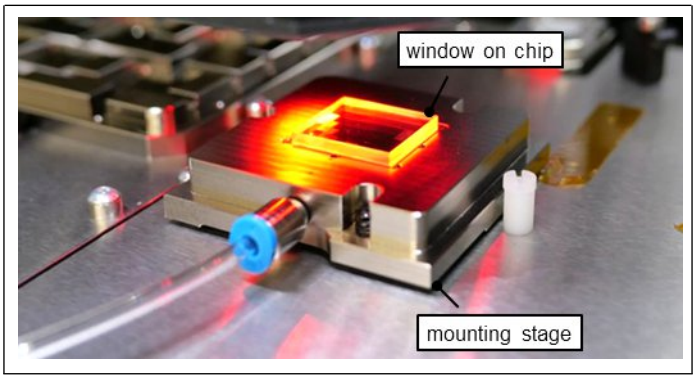


Figure 54: Mounting stage on die bonder machine table with window placed on chip

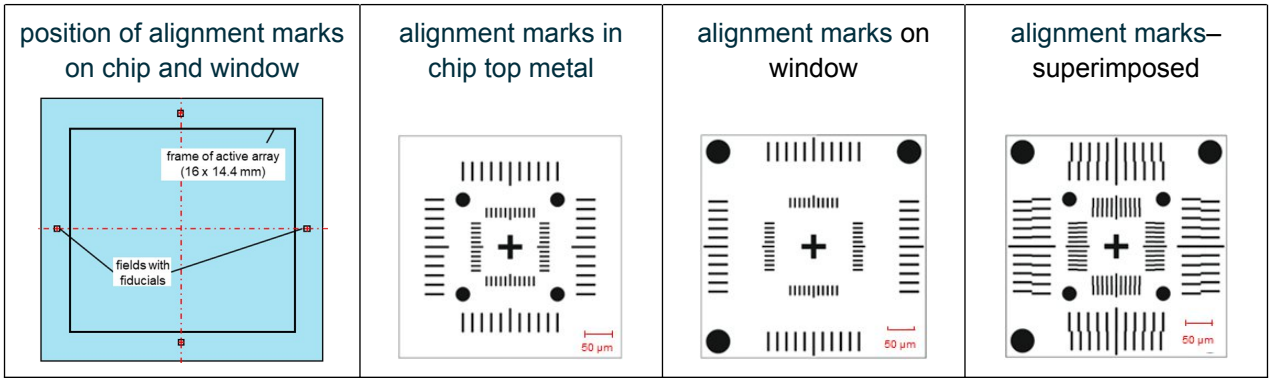


Figure 55: Layout of alignment marks for precise position detection of AHS and window: (a) position on the chip, (b) alignment marks on chip, (c) … on window, (d) combined alignment marks after assembly

The process development for window assembly was carried out during a project phase, where the final chip module had not been available yet. Using test devices for chip and window Fraunhofer IPMS managed to obtain promising results with a lateral placement accuracy in the range of a few microns. Evaluation of the obtained precision can be done by using the bonder image recognition software or even with a simple light microscope by analyzing the integrated vernier scales on chip and window. Figure 56 (a), (b) shows the combined alignment marks from chip and window after assembly. The difference in the step size of the scale from chip to window is 1 micron for the outer scale and 0.2 micron for the inner scale. An evaluation of placement accuracy in the micron scale is possible.

The work on the window assembly was frozen at a certain point in the project, where the project consortium was reorganized and goals were shifted a bit. Fraunhofer IPMS hopes to continue the

work in a follow-up project and to equip real AHS devices and to characterize the placement accuracy under wider thermal conditions.

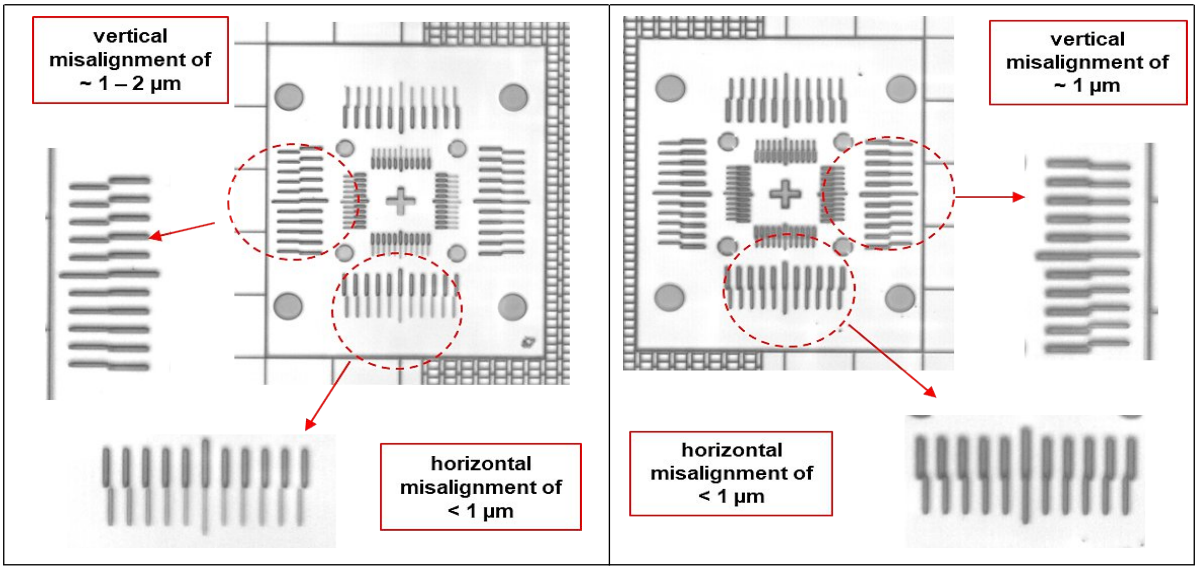


Figure 56: Picture of combined alignment marks from chip and window after assembly. Precise evaluation by use of integrated vernier scales on both partners: (a) alignment marks and vernier scales from central left position and (b) from central right position

Chapter 5 MMA Characterization

Prior to the fabrication of the final MEMS actuator on the CMOS, two types of passive devices (movable actuators without CMOS backplane) were designed for actuator and technology development and as a proof of concept.

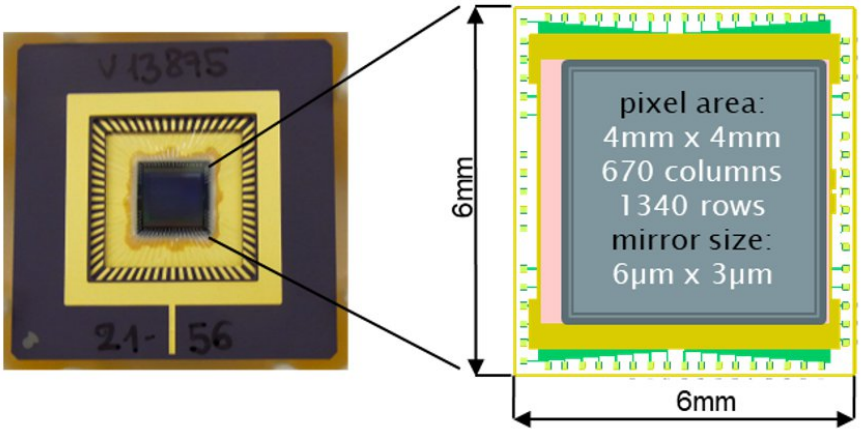


Figure 57: Small passive MMA as a first proof of concept

For the small passive devices (Figure 57), various design options were tested, including different spring and comb geometries, spring thicknesses and gaps. The straight-spring (S-spring) type showed the best performance in the characterization tests, and its fabrication process was more successful than other designs. In the second phase of the project full-size passive samples with 2400 rows and 4000 columns were designed and developed featuring the most suitable design variants, see Figure 58.

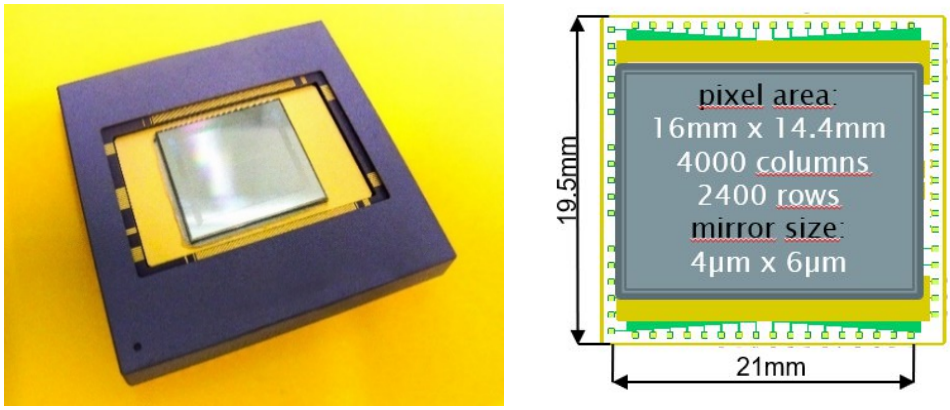


Figure 58: full-size passive MMA in a ceramic package and its general layout

By means of the Scanning Electron Microscope (SEM), a detailed examination of the MEMS fabrication process was conducted. Illustrative pictures of the straight-spring actuator are depicted in Figure 59.

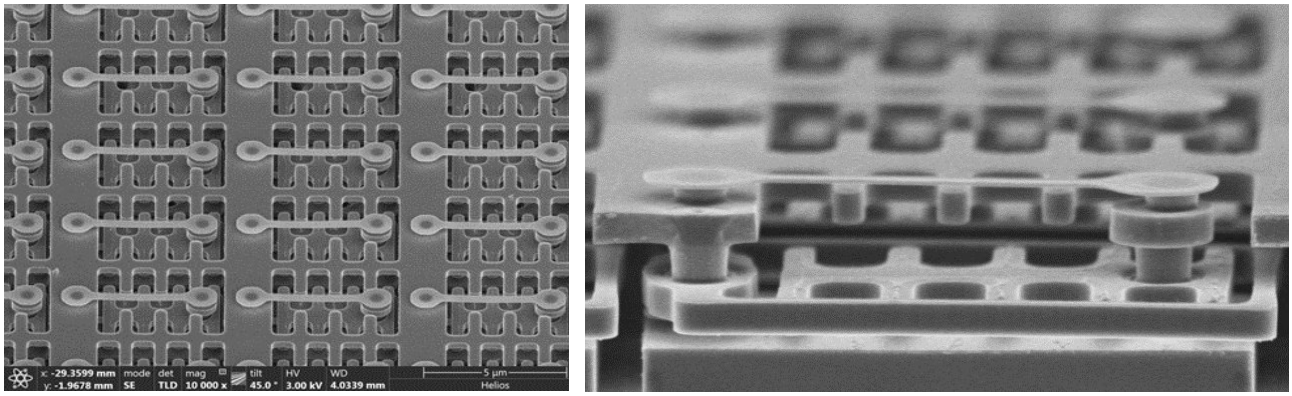


Figure 59: SEM images of actuator: 4-fingers comb (left) and 5-fingers comb and shield ring (right)

The main tool employed for the electro-opto-mechanical characterization is the White Light Interferometer (WLI). The WLI-setup in shown in Figure 60.

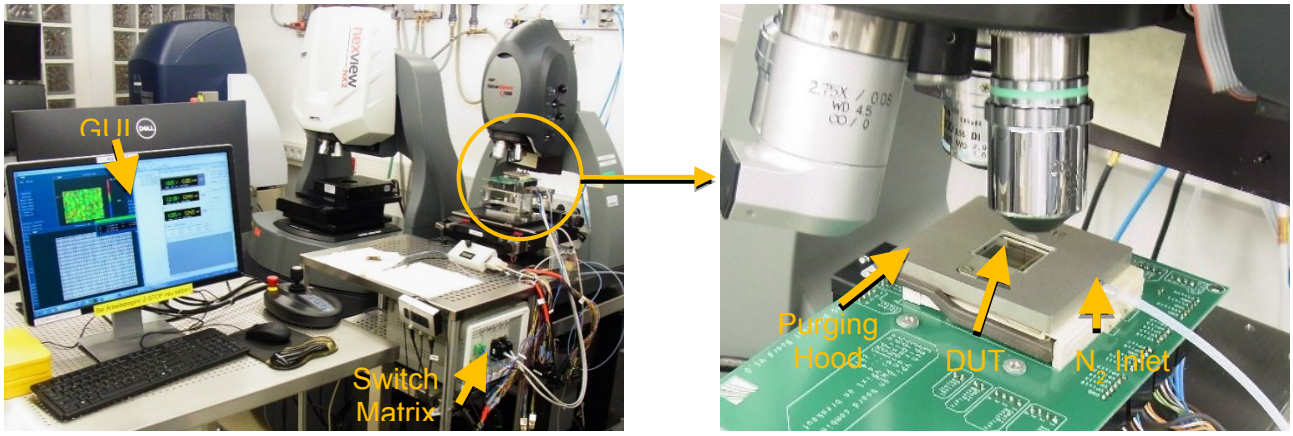


Figure 60: Measurement laboratory setup for full-matrix passive samples

In order to evaluate the dynamic behaviour of the micromirrors of the passive devices, the resonance frequency and damping for single actuators were analyzed by means of laser-doppler vibrometry measurements (Polytec MSA-500). The results can be seen in Figure 61 and Figure 62. The mirrors were addressed with a square wave signal of 6 V with a frequency of 10 kHz and a duty cycle of 30%.

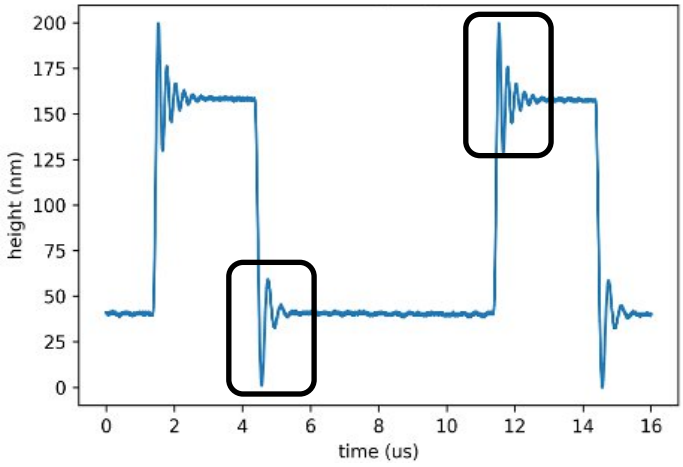


Figure 61: Dynamic mirror behaviour of single mirror

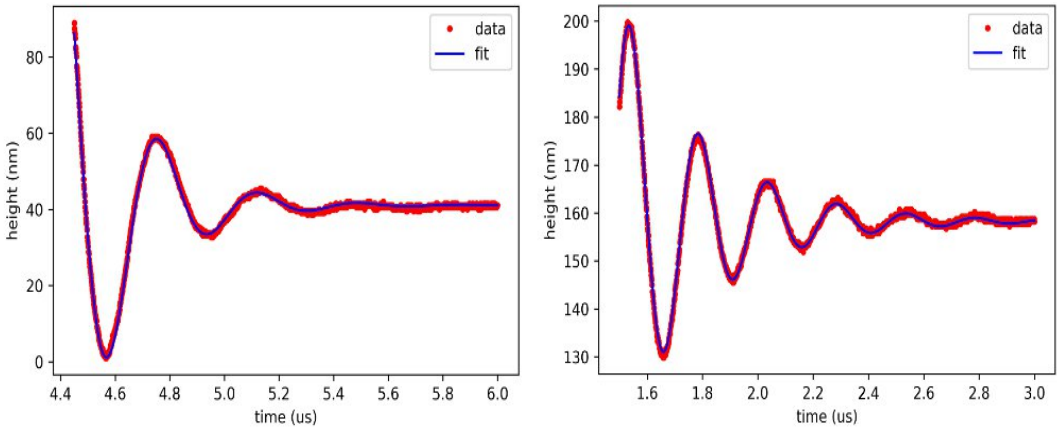


Figure 62: close-ups for downward movement (left) and for upward movement (right)

Although we could not address the active samples (MEMS with CMOS backplane) as planned with the specific electronic system, we decided to develop a simplified approach to check at least the quality of the MEMS part in the micromirrors arrays. In that way we proved that most of the mirrors are working as expected. In the height profile of two WLI measurements are showed: on the left side the voltage applied to the stator is 0V and on the right side, is 8V. The displacement achieved at 8V is more than 400nm relative to a non-moving mirror.

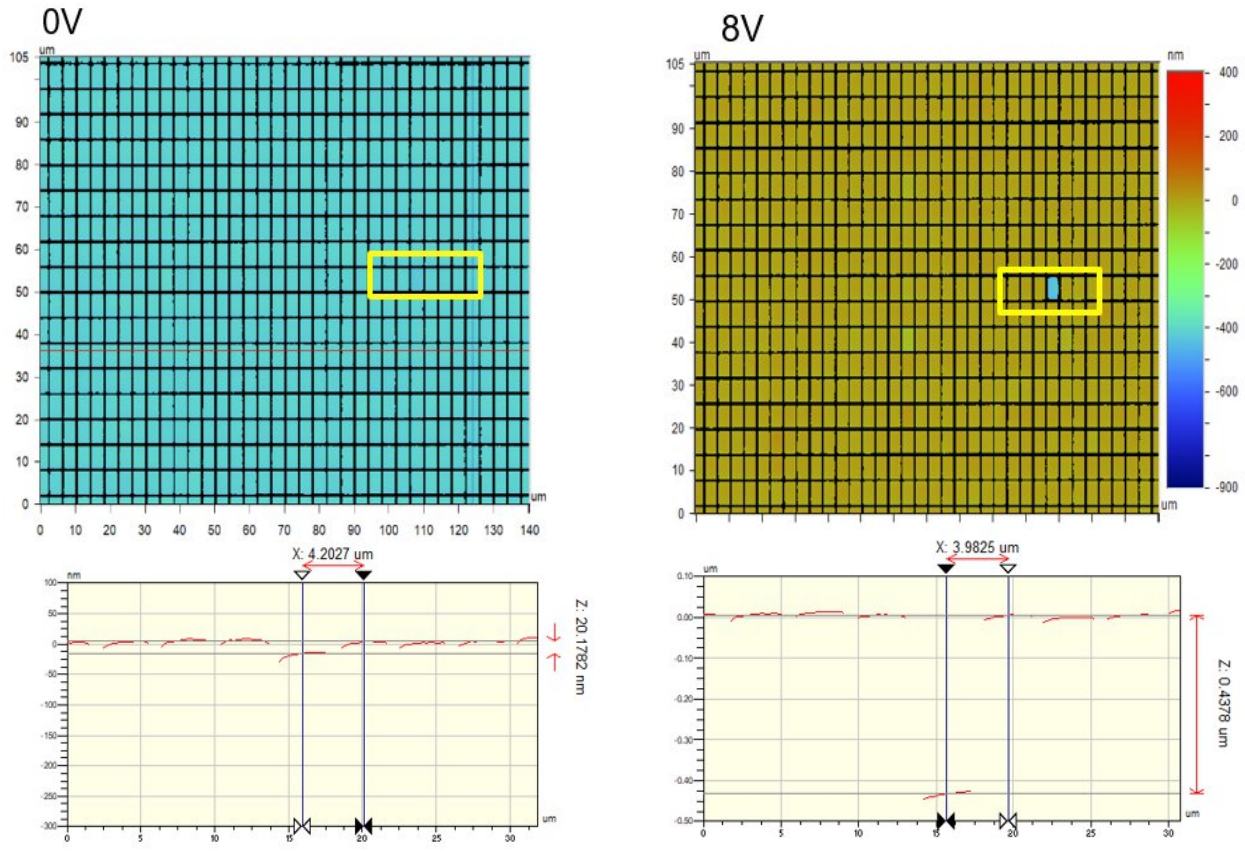


Figure 63: Height profiles of a WLI Measurement Field

The response curve achieved fulfil the requirements in terms of deflection to modulate RGB light as specified (see Figure 64) and confirms the simulation FEM results.

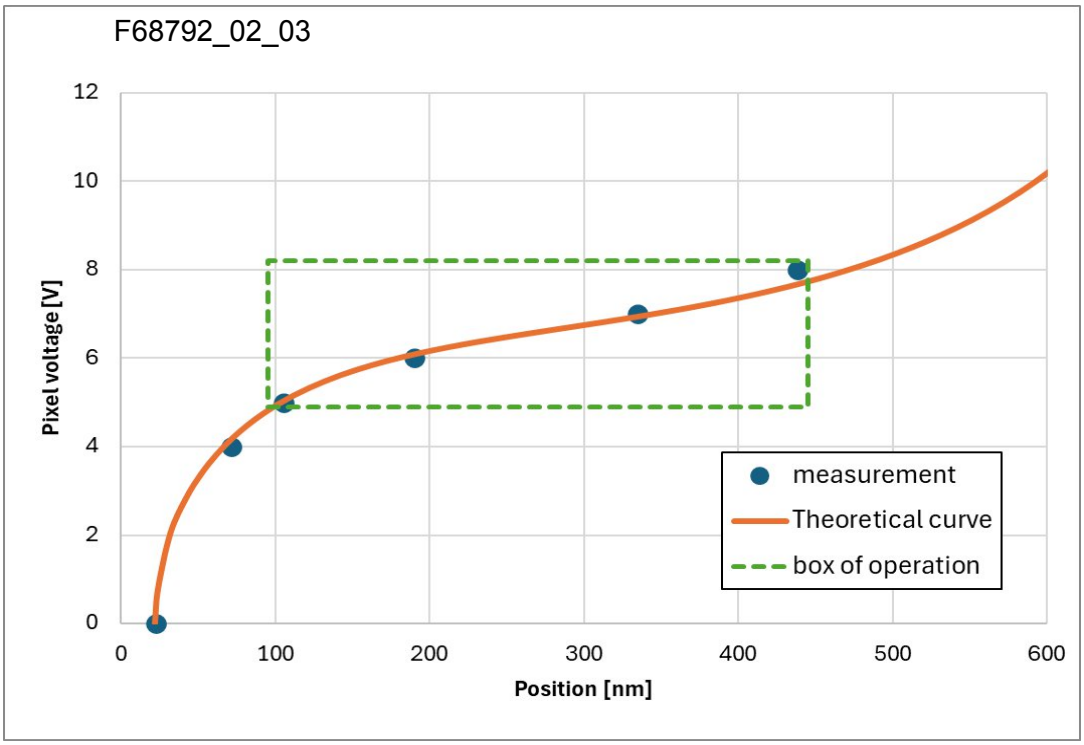


Figure 64: AHS-response curve of a single mirror under passive addressing

Chapter 6 Summary and Conclusion

Computer generated holography (CGH) offers the best possible solution for very interesting applications like virtual, augmented and mixed reality. To get the images from the computer into the real world, spatial light modulators (SLMs) are required that fulfil very demanding specifications. Unfortunately, none of the SLMs available at the start of this project could meet this challenge fully. We therefore developed a novel kind of MEMS (micro-electro-mechanical system) SLM especially for CGH applications. The challenge is to modulate the phase of incoming coherent light with millions of individually controllable pixels at a high frame rate. The pixels have to be only a few micro-meters in size for acceptable diffraction angles and still have a stroke range of half the wavelength of visible light, about 350nm. Within this range, each pixel needs to be set very precisely to one of many deflection levels at frame rates of more than one kHz.

This report discusses the challenge and our solution: an innovative MEMS comb drive actuator array, monolithically integrated on top of a CMOS backplane. FEM simulations show that a properly optimized comb drive allows for the required large stroke in quite small pixels with rather small addressing voltages, while almost completely suppressing any actuator cross talk. The response curve is simulated to be much closer to linear than for the parallel-plate electrostatic actuators that are much more common for phase modulating mirror arrays. This results in a superior precision of deflection and therefore superior image quality. This basic actuator principle has been transferred to a design that actually can be manufactured with the wafer processing machines available and also is quite in-sensitive to negative side effects.

The MEMS actuators and micro mirrors are manufactured on a wafer after the addressing circuitry has been made by a regular CMOS foundry (X-FAB). The MEMS is done layer-by layer in a clean room with processes similar to standard CMOS fabrication. In general, structural and sacrificial layers are deposited and patterned alternatingly and the sacrificial layers are planarized by CMP to get precise results. In a final step, the sacrificial layers are removed leaving the designed actuator structure free to move according to the electrostatic addressing. During the development of this process quite a few challenges had occurred, most of them related to extreme requirements on uniformity of CD, overlay and thickness. These challenges have been solved. A working process flow has been established and is reported on here.

The packaging of such MMAs needs to grant optical access to the mirrors, while at the same time protecting them from dust, humidity and other corrosive gases. It also needs to keep the active chip area flat over the whole operating temperature range. Therefore, we developed a process to integrate an optical window on the MMA chip, while the flatness and chip cooling is enabled by a rigid ‘heat slug’ beneath the chip. The electrical connections for high-speed data transfer and high precision operating and reference voltages are done by a high-end packaging substrate with very short wire bonds to the MMA chip, matched wires for best signal integrity, and integrated capacitors for voltage stability. The connection to the addressing electronics is done by an array of 1200 spring connectors. The packaging development thus fulfils all the requirements and is successfully completed.

The properties of MMA pixels were measured using white light interferometry and laser vibrometry. Response curves of recently fabricated samples show that a micro mirror displacement of 350 nm in piston mode is achieved allowing a full 2π phase modulation of RGB sources. For this an addressing voltage of 3.3 V, which is available from the CMOS backplane circuit, is sufficient, together with an additional global bias voltage of 3…4 V applied to the stator. First response curves of the proof-of-concept devices showed a good agreement with the FEM simulations. The actuator features a close-to-linear response within the designated range of operation just as expected from the simulations. Resonance frequencies around 270 kHz and damping factors of 0.2 were measured for the desired piston deflection mode. This also matches the FEM simulations very well and allows high frame rates compatible with time-sequential generation of RGB images.

More information and details on our results can be found in the papers that we have written and presented during the project. References to these are listed at the end of this report.

To conclude, the development of our new phase modulating micro-mirror array has been very successful, overcoming serious manufacturing and external issues. All the major goals have been achieved, and the first finished MMA chips show the feasibility of such high-resolution phase-modulating SLMs for computer generated holography. The achieved performance parameters are a very good starting point for fine-tuning the design and manufacturing process to develop a very high-quality commercial product. In addition, our MMA device and MEMS manufacturing process will also enable many other applications that may benefit from the fast and precise phase modulation by millions of pixels, like wave front shaping or quickly re-programmable diffractive optical elements (DOEs).

Chapter 7 List of Abbreviations

Abbreviation	Meaning
AHS	Active Holography SLM (MMA with CMOS backplane)
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
AR	Anti-Reflective
ASIC	Application Specific Integrated Circuit
CD	Critical Dimension – in lithography the features in the layout that are most important, often instead minimum feature size of a litho process
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing – process to planarize a surface
CVD	Chemical Vapour Deposition
FEM	Finite Element Method (in simulation) or Focus-Exposure Matrix (in lithography)
FOV	Field Of View
FPGA	Field Programmable Gate Array
HDP	High-Density Plasma (USG)
HF	Hydrofluoric Acid (Gas)
HTC	Holography Test Chip (small MMA with hard-wired pattern)
HUD	Head-Up Display
ILD	Inter Layer Dielectic ($Si0_2$)
LC	Liquid Crystal
LCD	Liquid Crystal Display
LCoS	Liquid Crystal on Silicon
LVDS	Low Voltage Differential Signal, standard electrical interface for data transfer
MEMS	Micro-Electro-Mechanical System
MMA	Micro Mirror Array
MR	Mixed Reality
PE	Plasma Enhanced (USG)
PHS	Passive Holography SLM (full-size MMA with hard-wired pattern)
PC	Personal Computer
RGB	Red-Green-Blue
RIE	Reactive Ion Etch
SA	Sub-atmospheric (USG)
SAC	SACrificial layer; MEMS layer that will be removed for the final device
SEM	Scattering Electron Microscope
SLM	Spatial Light Modulator (e.g. micro-display). We refer to the completely packaged device.
TRL	Technology Readiness Level
USG	Undoped Silica Glass

Chapter 8 List of References

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